Overshoot Improvement for Indirect Frequency Synthesizer Phase Locked Loop

Akram Al-Harasees, Ghadah O. Al-maaitah

Department of Electrical Engineering , Tafila Technical University
P.O. Box 179, 66110 Tafila-Jordan

***Abstract*—This paper presents an model for indirect frequency synthesizer, besides a simulation model by using ORCAD simulator. The main purpose in this paper is to make tradeoffs between settling time and overshoot of frequency synthesizer's output signal. The simulation results at 1KHz input frequency give a good a accuracy when the simulator behaviour is compared with a practical model. The proposed method has the capability to reduce the maximum overshoot of the PLL output signal. Finally some approval results in MATLAB model are presented.**

***Keywords*— CD4046B PLL, ORCAD, tradeoffs, settling time, overshoot, frequency synthesizer.**

I. INTRODUCTION

The mobile systems use frequency hopping technique for more security, and to protect the call from interruption. So there is a need to switch from one frequency to another in a fast way, and reducing the disturbances state during sudden change in frequency, frequency synthesizer is used widely to achieve this objective[1],[2]. Phase Locked Loop Frequency synthesizer (PLL FS) is used widely in wireless transceiver systems, and telecommunication technology. For instance; in receiver, the main purpose is to extract the information signal from modulated signal envelope. This can be done by generating a synthesized frequency at receiver to delete the incoming (received) carrier. PLL frequency synthesizer is appropriate to synthesize the carrier signal[3], [4].

Also, Frequency Synthesizer has been used as a source of wideband and stable frequencies, which can be generated from single source of frequency-or reference frequency (f_{ref}) . So it is found in many modern devices including clock generators, data recovery circuits, radio receivers [5], mobile telephones, walkie-talkies, satellite receivers, GPS. Frequency synthesizer is used to improve the efficiency of wireless LAN 802.11.a and 802.11b receiver, and to increase their band and data rates [6].

There are three types of frequency synthesizers: analog Direct frequency synthesizer, Indirect frequency synthesizer, and Digital direct frequency synthesizer. Analog Direct frequency synthesizer needs a lots of components with increasing the number of channels, so it is impractical to use this type in wireless communication systems such as GSM. Instead, indirect frequency synthesizer is used, this type uses a phase locked loop. PLL is the main part in frequency synthesizer, it was built since 1965 by using analog devices. Recently, with advancing of IC's, PLL components is integrated in a single IC, and become more efficient and reliable [5]. PLL is negative feedback circuit that compares a current value to a reference value to make the difference smaller as much as possible [4].

PLL represents an important method in the wireless communications revolution. The indirect frequency synthesizer is our approach in this paper**.** Unlikely of indirect frequency synthesizer, digital direct frequency synthesizer (DDFS) doesn't use feedback control to correct the difference in frequencies, since the VCO output in DDFS is always predictable and there is no variation from undesired excitations. DDFS uses the output of VCO directly as a final output frequency [1].

In this paper the key is in developing an appropriate model to simulate a practical model for indirect FS PLL, the result was obtained experimentally about maximum overshoot and settling time for the output signal of FS PLL . Device models and IC's simulators such as ORCAD can provide the circuit design with less time than that can be spent in laboratory, so faster and easier simulation results can be gained. Improvement trials are introduced to reduce the settling time and overshoot. Also, some results are obtained by using (Matlab) programs to make sure. In ORCAD simulator, we used CD4046B PLL as the main IC in simulation. This IC represents an equivalent circuit for MC14046B which have been used in a practical model.

Recently; fast settling and minimum overshoot are considered as important challenges in frequency synthesizer, multiple papers proposed a lot of methods to reduce these two challenges. [7] Proposed an application to obtain low power and fast settling time by developing a mixed signal LC VCO in PLL frequency synthesizer. The author in [8] proposed a fast lock in PLL frequency synthesizer by frequency hopping with mixed signal VCO and a direct circuit. [9] Introduced a new method to speed up the response of PLL, and then compared the result with PSB MATlAB. In [10] the author suggested a simulation for 2^{nd}-order and 3^{rd}-order PLL by using MATLAB SIMULINK model, and compared the results with mathematical model .[11] introduced a mixed signal VCO and a digital processor to switch between frequencies and then reducing the settling time. [12] Introduced adaptive phase-locked loop (PLL) architecture to discuss tradeoffs of multiple aspects (settling time, phase noise, and spurious signals). [13] proposed a method to reduce or eliminate ripple noise(overshoot) and increase synchronization speeds without the need for LPFs and complex controller implementations.[3] presented a new filter design method for PLL, the objective is to achieve small noise bandwidth, good transient response (small settling time, small overshoot, large gain and phase margins). [14] Proposed an adaptive control on the reference frequency and frequency divide ratio of PLL to achieve low noise and fast settling.

This paper organized as follow: in section II the PLL FS structure specification is introduced. In section III the simulation structure is performed. The simulation results is presented in Section IV, V introduces a conclusion.

II. PLL FS STRUCTURE:

Fig.1 shows the block diagram for the linear Indirect PLL FS in (S-domain). It contains phase detector (PD) with gain K_{PD}, Low Pas Filter (LPF), Voltage Control Oscillator (VCO) with gain K_{VCO} (Hz/V), and a fractional by N circuit arranged as a feedback loop[1] . By multiplying the reference frequency with multiplication factor N, the output frequency will be F_{out}= N. F_{ref} .

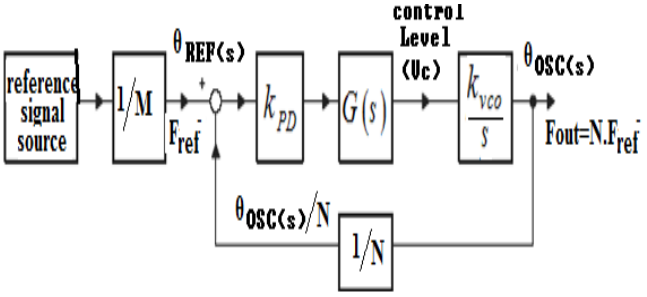

Fig.1 Frequency synthesizer Phase Locked Loop

The closed loop transfer function in s-domain for the circuit shown in Fig.1 is given as :

$$H(s)=\frac{K_{PD}K_{VCO}G(s)}{S+\frac{K_{PD}K_{VCO}G(s)}{N}} \qquad (1)$$

Where N is the division ratio. G(s) is the transfer function of low pass filter, K_{VCO} is the voltage controlled oscillator gain. K_{PD} is the phase detector gain and equal.

$$K_{PD}=\frac{(V_{OH}-V_{OL})}{4\pi} \qquad (2)$$

V_{OH} is the highest output of Phase detector (PD) voltage level, and V_{OL} is the lowest output of Phase detector voltage level.

Phase detector has two inputs; the incoming signal (reference frequency (F_{ref})), and the output of voltage control oscillator. F_{ref} is the frequency of oscillator after dividing it by the programmed value (M). Phase detector may be either analog or digital, for analog signal, phase detector can be as a multiplier circuit or modulator circuit. For digital signal, phase detector can be as an OR-gate, XOR-gates, RS flip-flop, 3-state buffer, or phase frequency detector [1]. PD compares the input frequency with the output of VCO signal after dividing it by a programmed value (N) at frequency divider circuit [4]. Phase detector detects the phase difference between two inputs frequencies, and produces a voltage level according to this difference [15]. Output of Phase detector or the result of comparison (or multiplication) has high frequency terms and low frequency terms, this output is smoothed by Low Pass Filter (LPF) to eliminate high frequencies [4],[3], output of low pass filter contains the difference in the frequencies and the phases between input signal and feedback signal, this difference or error will control the VCO oscillating, when there is no error, then the VCO will produce the center frequency which ensures the PLL to be in lock range. If there is some difference, VCO will produce a frequency according to this difference, here, PLL lacks the lock range, and the operating frequency will be changed [4]. Therefore PLL try to minimize the difference (error) in phase and frequency with respect to incoming signal, and to make this error as small as possible until the circuit will be in lock range. VCO is a resonance (tuned) circuit has a gain $K_{VCO,}$ and can oscillate at resonant frequency, this frequency can be changed by Varactor diode which acts as capacitance, and this capacitor is varied by control voltage from LPF. Fig.2 shows the passive LPF.

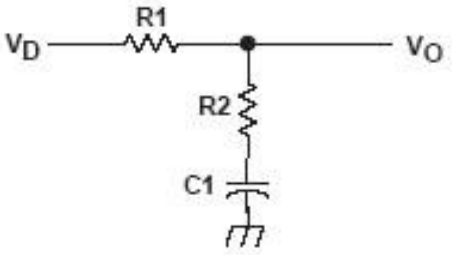

Fig.2 : passive Low Pass Filter

The LPF has first order transfer function G(s)

$$G(s)=\frac{Vo}{V_D}=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)} \qquad (3)$$

Where τ_1= R_1C_1, τ_2= R_2C_2 are the time constants of the loop filter. By substituting (3) into (1), the PLL FS transfer function becomes :

$$H(s)=\frac{1+s\tau_2}{(\tau_1+\tau_2)s^2+(\frac{N+K\tau_2}{NK})s+\frac{1}{N}} \qquad (4)$$

$K=K_{PD}K_{VCO}$ is the overall gain of closed loop of FS PLL.

From equation (4), it is clear that if the frequency is switched from hop to another by changing N factor, then there will be a sudden change in output frequency, this change causes a phase disturbances at output signal, and there is a settling time required to reach a new steady state. Besides, an overshoot will appear until return to steady state.

Equation (4) can be written in term of damping factor ξ and natural frequency ω_n :

$$H(s)=\frac{1+(\frac{2\xi}{\omega_n}-\frac{N}{K})s}{(\frac{1}{\omega_n^2})s^2+(\frac{2\xi}{\omega_n})s+1} \qquad (5)$$

Where

$$\xi = \frac{1 + K\tau_2}{2\sqrt{N(\tau_1 + \tau_2)K}} \qquad (6)$$

And

$$\omega_n = \sqrt{\frac{K}{N(\tau_1 + \tau_2)}} \qquad (7)$$

ξ represents measure of stability , usually it is selected to be between 0.6-0.8.

It is expected that the output frequency determines two things [1]:

1) The settling time which is become too slow or fast by time constant of loop filter (τ).
2) The damping of the loop (or overshoot) when the loop accept sudden change in frequency.

III. SIMULATION STRUCTURE:

A. *Practical Structure:*

The practical model of PLL FS is shown in Fig.3[1], this circuit operates in laboratory and give the results which are compared with a simulation results by using ORCAD.

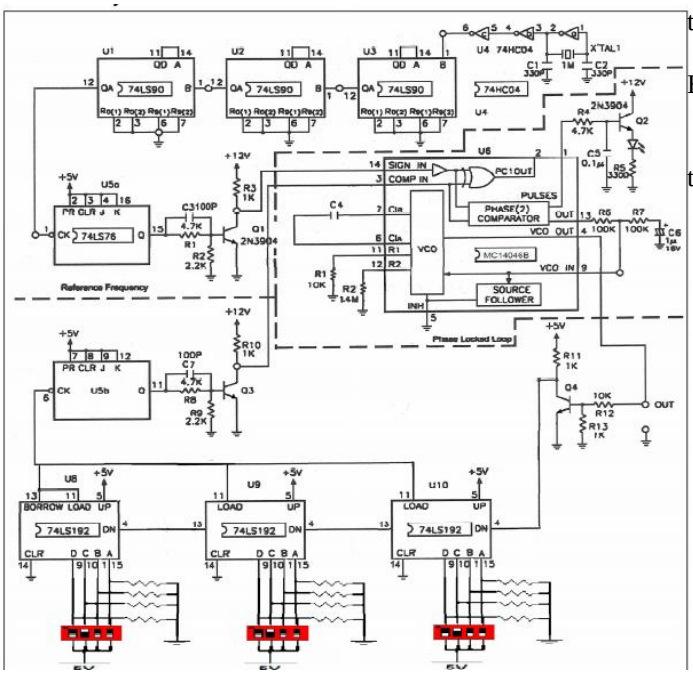

Fig.3 PLL Frequency Synthesizer Circuit practical Schematic

The circuit in Fig.3 shows three section:

- Reference frequency section.
- PLL section.
- Divide-by-N section

The Reference frequency section consists of crystal oscillator (XTAL 1MHz), and frequency dividers (74HC04) which divide crystal oscillator frequency by 1000 to obtain 1kHz as a reference frequency (F_{ref}). In practical consideration, many types of FS cannot operate over a wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition, it is hard to make a high frequency VCO that operates over a wide range. However, in most systems where the synthesizer is used, we don't operate over a huge range, but rather a finite number over some defined range of frequencies, such as a number of radio channels in a specific band.

The second section is Phase Locked Loop (PLL) as a single IC. The final section is (BY N) section which produce a fractional by N frequency. Three BCD counters (74LS192) with dip switches divide the output frequency.

Each stage of synchronous up/down decade counters (SN74192) is used as a down counter whose outputs are preset by 3 BCD (4-bit) dip switches outputs and load input signal. When a low (0) inputs for BCD presented at load control input (pin 11), the BCD inputs (pins 15, 1, 10, and 9) will be loaded into the decade counter. When input pulses reach at the down-count input (pin 4), the counter counts down and the borrow output (pin 13) produces a pulse as the counter underflows. For example, the three down counters U8, U9, and U10 are preset to 2, 1, and 3 by the hundreds, tens, and units 3 BCD switches, respectively. Each input pulse to the units counter U10 pin 4 results in a decrement of counter values. After 213 input pulses, an output pulse appears at U8 pin 13 (borrow output). The borrow output pulse (low) is connected to the load inputs of these three counters to reload the value 213 into the counters and then the counting sequence runs repeatedly [1].

B. *Simulation Model:*

Before starting the simulation in ORCAD, we have to do three steps:

- Drawing the schematic for simulation.
- Selecting the reference oscillator, and setting the values of its parameters.
- Determining the linear region of operation for VCO .
- set up the profile of simulation by calling new simulation profile in NEW SIMULATION PROFILE window, and selecting the analysis type which can be as a DC analysis , ac analysis, or transient analysis. After then select the RUN time which clarify the scale of time in the result.

Fig .4 shows the block diagram of the PLL FS which is designed by ORCAD, CD4046B is used as an equivalent for a practical model of PLL.

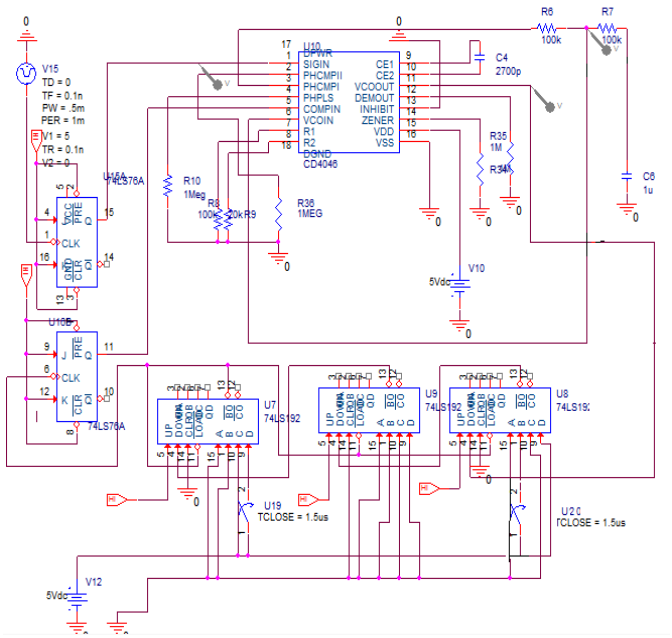

Fig.4 simulation model in ORCAD for PLL FS

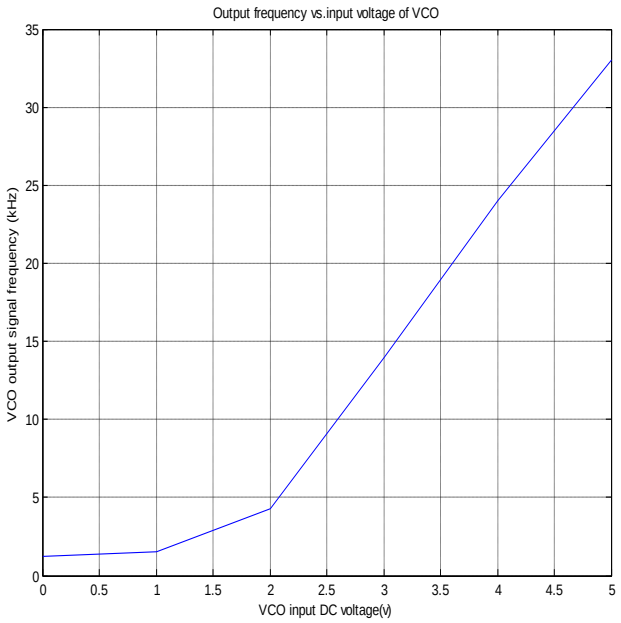

Fig.5 output frequency vs Input voltage characteristic of VCO

CD4046B contains a VCO and Phase comparator. Two inputs at PD, input signal at pin1(SIGN) and feedback signal at pin 5(COMPIN) . Output of comparator at pin2 (PCOMPll) enters into loop filter at R6, R7, C6. (VCOOUT) output signal at pin 11 enters into frequency divider BCD (74LS192).

The selected reference oscillator in our simulator which produces the desired frequency is a VPULS function, so there is no need to use the crystal oscillator which is used in practical model to obtain the source signal at 1MHz, and then dividing this frequency by using a serial circuits of 74LS90 IC,s until to reach at 1kHz frequency. There are some parameters in VPULSE is adjusted, V1=5v, V2= zero, period (PER)= 1ms, and the pulse width (PW)= 0.5ms. These parameters will produce a 1KHz square wave signal.

The VCO must operate in the linear region; this ensures that PLL approximately will be in lock range. This step can be done by applying DC voltage sources on CD4046B and disconnect any other input signals, for each value of the applied DC voltages there is an output frequency, this can be shown in Fig.5. From Fig.5, K_{VCO} gain can be calculated [1] as:

$$K_{VCO} = \frac{(F_{max} - F_{min})}{(V_{max} - V_{min})} \qquad (8)$$

$$= 8.57\text{KHz})/V$$

Time Domain (Transient analysis) is selected in ORCAD, since the sudden change in frequency from value to another gives a transient disturbance before returning to a steady state.

Output of VCO enters the loop filter, in our model it consists of R6,R7, and C6. If the reference frequency leads the feedback signal, the difference will charge the capacitance C6, but if reverse C6 will be discharged. If two inputs are in the same phase, then C6 holds the charge. This can be shown in Fig.6.

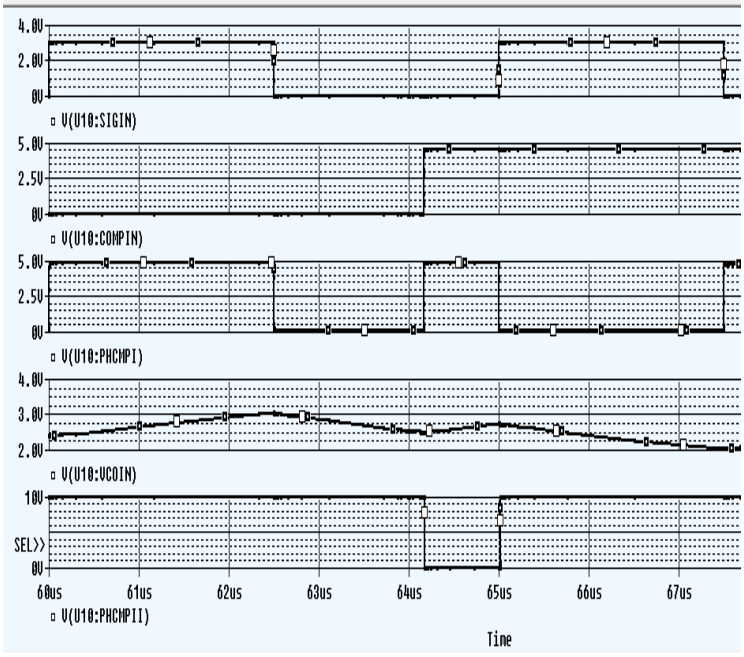

Fig.6 the output signals from each stage in PLL FS

IV. Simulation Results

By using (5), and when ξ equal 0.7, Fig.7 shows the output frequency versus time. When a sudden change in frequency occurs, the output signal tries to settle to the steady state value after a settling time ts:

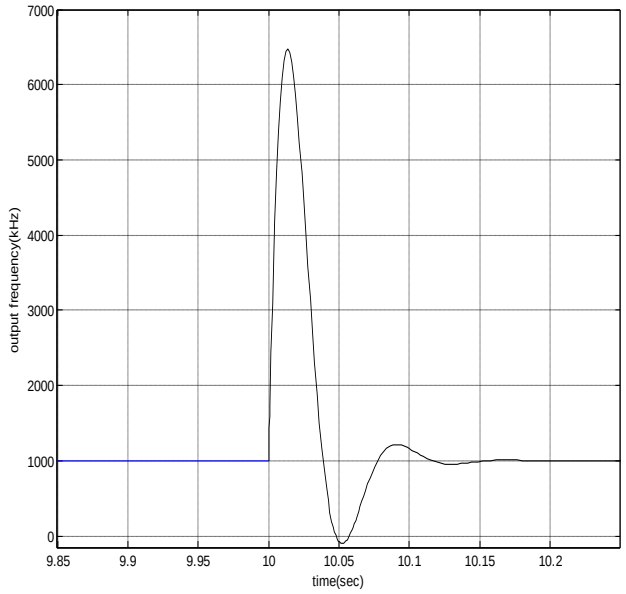

Fig.7 Frequency versus time at output signal.

Now Fig.8 and Fig.9 introduce the transient response of the circuit model in Fig.4. These results are obtained at VCO output. From these figures we obtain the settling time which is from the beginning of the maximum overshoot. The sudden change in the input frequency can be established by using 3BCD and switches to change the frequency from 200 KHz to 300 KHz(Fig.8), and from 600 KHz to 700 KHz (Fig.9).

Based on these results, there are two of the possible transient response captures for different values of N factor. Although N factor changes from 200-300 in Fig.8, while it changes from 600-700 in Fig.9, the result of the output signal still approximately has the same maximum overshoot and settling time. Changing the frequency from 200 KHz to 300 KHz in Fig.8 gives 335mv maximum overshoot with 0.01 µsec settling time. And changing from 600 KHz to 700 KHz in Fig.9 gives 300mv maximum overshoot with settling time equal 0.01µsec

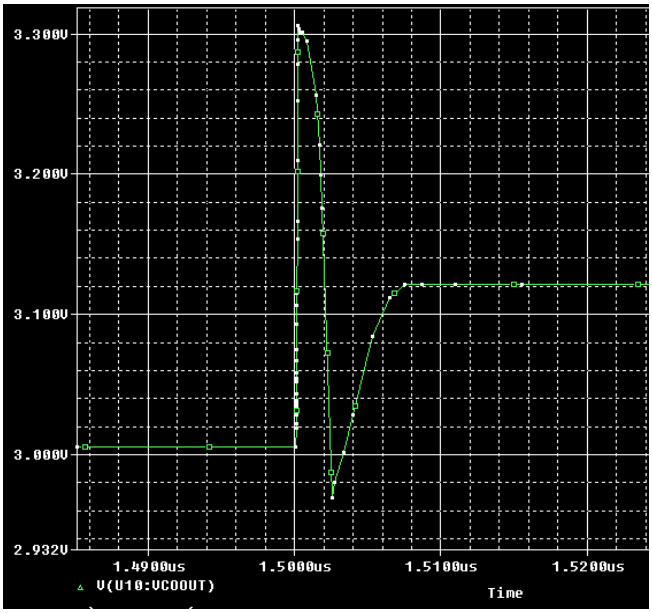

Fig.8 PLL FS transient response capture for N= 200-300

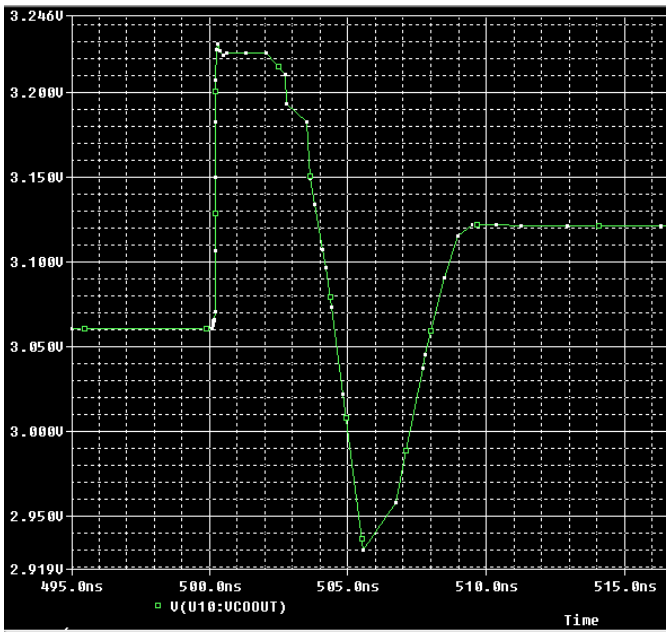

Fig.9 PLL FS transient response capture for N= 600-700

To improve the maximum overshoot, an external capacitor (Ce) is connected between VCO input at pin6 and ground , the value of capacitance is calculated as:[1]

$$Ce=kC_6 \quad (9)$$

Where Ce is the external capacitor, C_6: is the LPF connected capacitor in the simulation model circuit. k is the improvement factor and equal[1]

$$k=\frac{1}{1-\xi} \quad (10)$$

We assumed that the required ξ is 0.9, so as to be close as possible to the critical value which is equal 1 [16] . Ce will be 10µF.

Fig.10 shows the transient response of the frequency synthesizer with connecting the external (10 µF) capacitor. By using external capacitor maximum overshoot becomes 100mv ,but the settling time equal 0.024µsec.

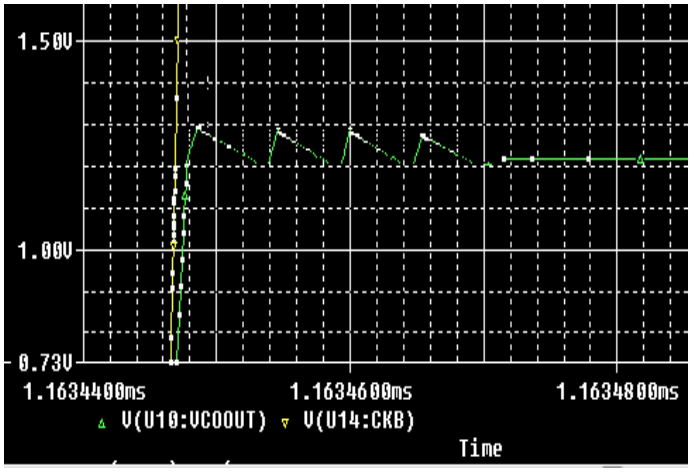

Fig.10 transient response with improvement element

V. CONCLUSIONS

This paper proposed a PLLFS model utilizing the multi programmable divider, which can attain a higher speed; lock up time (settling time) or lowering the maximum overshoot by increasing the loop gain which is occurred as a result of adding external capacitor to the lag-lead loop filter.

Based on the results, approximately changing the division factor N doesn't change the maximum overshoot or settling time. That means Changing the frequency from one value to another causes some disturbance but this disturbance approximately has same settling time and maximum overshoot level.

Adding a capacitor element (Ce) decreases the maximum overshoot by 70%, while there is an increasing in settling time. Here, there are two tradeoffs (settling time and maximum overshoot) according to the kind of application of PLLFS which is needed. In future work we will try to minimize both overshoot and settling time to have optimal performance of indirect frequency synthesizer PLL.

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Akram Al-Harasees received his BSC in Electrical engineering\Communication and electronic Engineering from Yarmouk University, Jordan, 1987. And M.SC in Communication Engineering from Mutah University, Jordan ,2010. Eng. Al-Harasees is specialized in electrtonic and communication Engineering. He is Faculty member in TTU in Jordan, since 2010. His areas of research include electronic design.

Ghadah O. Al maaitah received her BSC and MSC in Communication Engineering from Mutah University, Jordan , in 2000 and 2008, respectively. Eng. Al-maaitah is specialized in communication Engineering. she is Faculty member in TTU in Jordan, since 2008.

Her areas of research include wireless communication systems, and electronic design.