Symbolic Simulation by Nodal Method Of Complementary Circuitry

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***Abstract*— The initial values of transient response of the RLC circuit are mainly expressed in terms of branch state variables which may be of both the inductor current and capacitor voltage or either. When transient response is initiated from steady state, these state variables are direct consequence of steady state response. In this paper it is shown that when time domain nodal equation representing the transient response is translated to laplace domain, a guided substitution of the initialization quantities in terms of steady state nodal voltages would led to well structured symbolic nodal equation which simplifies symbolic transient response simulation.**

***Keywords*— Transient response, state variables, laplace domain, steady state and symbolic nodal equation.**

I. INTRODUCTION

Some of the tasks that cannot be solved effectively by conventional simulation have become tractable by extending the simulation to operate a symbolic domain. Symbolic simulation involves introducing an expanded set of signal values and redefining the basic simulation functions to operate over this expanded set. This enables the simulator evaluate a range of operating conditions in a single run. By linearizing the circuits with lumped parameters at particular operating points and attempting only frequency domain analysis, the program can represent signal values as rational functions in the s (continuous time) or z (discrete time) domain and are generated as sums of the products of symbols which specify the parameters of circuits elements [1 – 4]. Symbolic formulation grows exponentially with circuit size and it limits the maximum analyzable circuit size and also makes more difficult, formula interpretation and its use in design automation application [5 – 11]. This is usually improved by using semisymbolic formulation which is symbolic formulation with numerical equivalent of symbolic coefficient. Other methods of simplification include simplification before generation (SBG), simplification during generation (SDG), and simplification after generation (SAG) [12 – 19].

Symbolic response formulation of electrical circuit can be classified broadly as modified nodal analysis (MNA) [20], sparse tableau formulation and state variable formulation. The state variable method were developed before the modified nodal analysis, it involves intensive mathematical process and has major limitation in the formulation of circuit equations. Some of the limitations arise because the state variables are capacitor voltages and inductor current [21]. The tableau formulation has a problem that the resulting matrices are always quite large and the sparse matrix solver is needed. Unfortunately, the structure of the matrix is such that coding these routine are complicated. MNA despite the fact that its formulated network equation is smaller than tableau method, it still has a problem of formulating matrices that are larger than that which would have been obtained by pure nodal formulation [22]. In this paper a new nodal analytical method is introduced which may be used on linear or linearized RLC circuit and can be computer applicable and user friendly. The simplicity of the new transient nodal formulation lies in the fact that minimal nodal index is enough to formulate transient equation and also standard method of building steady state nodal admittance bus is just needed to build the two formulated admittance buses that are required to formulate transient nodal equation. Simplicity, compactness and economy are the advantages of the newly formulated nodal equation.

II. NEW NODAL TRANSIENT ANALYSIS

The new nodal method sees a transient network in frequency domain as one that sets up complementary circuit by the initial dc quantities at the inception of transient. With this nodal method, the complementary circuit sets its resultant residual quantities (transient dc current source) which complement the nodal laplace domain current source equivalent. The resultant effect of the initial dc quantities and the transient current source on nodal transient circuit equation (1) is setting up of two identifiable admittance diagrams. One admittance diagram is the normal laplace transformed admittance diagram of the original circuit elements, in this paper it is called the auxiliary transient admittance diagram. The other admittance diagram is due to none - zero transient initialization effect of the storage elements and it is called the complementary transient admittance in this paper.

$$Y(s)V(s) - J(s) = Y_c(s)V_c(s) - J_c(s) \qquad (1)$$

Where Y(s) is the Auxiliary admittance bus, that is s – domain equivalent of steady state nodal admittance matrix, $Y_c(s)$ is the s – domain complementary admittance bus, of storage element driving point impedance bus due to dc nodal voltage at transient inception, V(s) is the laplace nodal voltage, J(s) is the laplace nodal current source vector and $J_c(s)$ is the initial dc transient nodal current source vector due to constitutive effect of steady state branch source voltage on the branch source voltage (9).

A. New Transient Nodal Formulation Derivation

The derivation of these two admittance buses and the formulation of the new s – domain nodal equation by method of complementary circuitry are thus as follows,

For node 1

Consider a three node circuit in fig 1, the generalization of nodal analysis of n – th node may be demonstrated by forming equations of Kirchhoff's current law at the three various nodes, thus at node 1

$$i_1 + i_4 - i_5 = 0 \quad (2)$$

For i_4

The constitutive relation of the branch elements is as follows

$$V_1(t) - E_4(t) - V_2(t) = R_4 i_4(t) + L_4 \frac{d}{dt} i_4(t) + \frac{1}{c_4} \int i_4(t) \quad (3)$$

taking the laplace transform of equation (3),

$$V_1(s) - E_4(s) - V_2(s) = [R_4 + sL_4 + \frac{1}{sC_4}] i_4(s) - L_4 i_4(0) + \frac{V_{C4}(0)}{s} \quad (4)$$

but

$$V_{C4}(0) = \frac{i_4(0)}{s_1 C_4} \quad (5)$$

$$i_4(0) = [V_1(0) - E_4(0) - V_2(0)] Y_4(s_1) \quad (6)$$

$$\Rightarrow$$

$$V_{C4}(0) = [V_1(0) - E_4(0) - V_2(0)] \frac{Y_4(s_1)}{s_1 C_4} \quad (7)$$

Substituting equation (7) in (4) and simplifying to get,

$$i_4(s) = [V_1(s) - V_2(s)] Y_4(s) - E_4(s) Y_4(s) + [V_1(0) - V_2(0)] Y_{(C)4}(s) - E_4(0) Y_{(C)4}(s) \quad (8)$$

where

$$Y_{(C)k}(s) = Y_k(s) Y_k(s_1) Z_{(C)k}(s), \quad (9)$$

$$Y_k(s) = \frac{1}{R_k + sL_k + \frac{1}{sC_k}}, \quad (10)$$

$$Y_k(s_1) = \frac{1}{R_4 + s_1 L_4 + \frac{1}{s_1 C_4}} = \frac{1}{R_4 + j\omega \cdot L_4 + \frac{1}{j\omega \cdot C_4}} \quad (11)$$

$$Z_{(C)k}(s) = [L_4 - \frac{1}{s s_1 C_4}], \qquad s_1 = j\omega \quad (12)$$

For i_1

Similarly,

$$i_1(s) = V_1(s) Y_1(s) - E_1(s) Y_1(s) + V_1(0) Y_{(C)1}(s) - E_1(0) Y_{(C)1}(s) \quad (13)$$

For i_5

Similarly

$$i_5(s) = [V_1(s) - V_3(s)] Y_5(s) - E_5(s) Y_5(s) + [V_1(0) - V_5(0)] Y_{(C)5}(s) - E_5(0) Y_{(C)5}(s) \quad (14)$$

The sum of currents flowing unto node 1 may be obtained by adding equation (8), (13) and (14) thus

$$V_1(s)[Y_1(s) + Y_4(s) + Y_5(s)] - V_2(s) Y_4(s) - V_3(s) Y_5(s) - [E_1(s) Y_1(s) + E_4(s) Y_4(s) - E_5(s) Y_5(s)] = -\{V_1(0)[Y_{(C)1}(s) + Y_{(C)4}(s) + Y_{(C)5}(s)] - V_2(0) Y_{(C)4}(s) - V_3(0) Y_{(C)5}(s) - [E_1(0) Y_{(C)1}(s) + E_4(0) Y_{(C)4}(s) - E_5(0) Y_{(C)5}(s)] \} \quad (15)$$

For Node 2

Similarly, the Kirchhoff's current equation for node 2 may be written as follows

$$V_2(s)[Y_2(s) + Y_4(s) + Y_6(s)] - V_1(s) Y_4(s) - V_3(s) Y_6(s) - [E_2(s) Y_2(s) - E_4(s) Y_4(s) - E_6(s) Y_6(s)] = -\{V_2(0)[Y_{(C)2}(s) + Y_{(C)4}(s) + Y_{(C)6}(s)] - V_1(0) Y_{(C)4}(s) - V_3(0) Y_{(C)6}(s) - [E_2(0) Y_{(C)2}(s) - E_4(0) Y_{(C)4}(s) - E_6(0) Y_{(C)6}(s)] \} \quad (16)$$

For Node 3

Similarly, the Kirchhoff's current equation for node 3 may be written as follows

$$V_3(s)[Y_3(s) + Y_5(s) + Y_6(s)] - V_1(s) Y_5(s) - V_2(s) Y_6(s) - [E_3(s) Y_3(s) + E_5(s) Y_5(s) + E_6(s) Y_6(s)] = -\{V_3(0)[Y_{(C)3}(s) + Y_{(C)5}(s) + Y_{(C)6}(s)] - V_1(0) Y_{(C)5}(s) - V_2(0) Y_{(C)6}(s) - [E_3(0) Y_{(C)3}(s) + E_5(0) Y_{(C)5}(s) + E_6(0) Y_{(C)6}(s)] \} \quad (17)$$

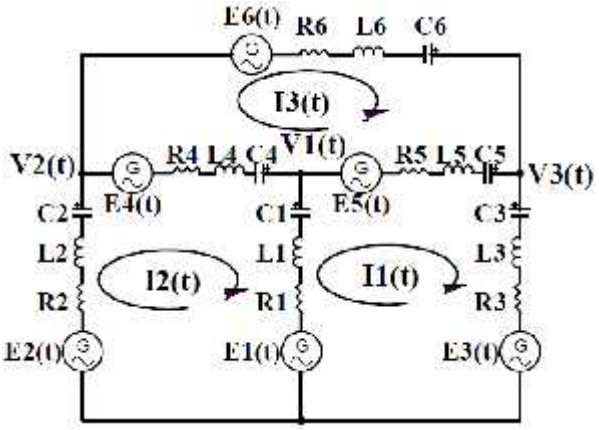

Figure 1: Three node, three mesh RLC electrical circuit.

Equation (15), (16) and (17) are combined to get the transient nodal equation for fig 1 circuit as follows

$$\begin{pmatrix} Y_{11}(s) & Y_{12}(s) & Y_{13}(s) \\ Y_{21}(s) & Y_{22}(s) & Y_{23}(s) \\ Y_{31}(s) & Y_{32}(s) & Y_{33}(s) \end{pmatrix} \begin{pmatrix} V_1(s) \\ V_2(s) \\ V_3(s) \end{pmatrix} - \begin{pmatrix} J_{(N)1}(s) \\ J_{(N)2}(s) \\ J_{(N)3}(s) \end{pmatrix} = \begin{pmatrix} Y_{(c)11}(s) & Y_{(c)12}(s) & Y_{(c)13}(s) \\ Y_{(c)21}(s) & Y_{(c)22}(s) & Y_{(c)23}(s) \\ Y_{(c)31}(s) & Y_{(c)32}(s) & Y_{(c)33}(s) \end{pmatrix} \begin{pmatrix} V_1(0) \\ V_2(0) \\ V_3(0) \end{pmatrix} - \begin{pmatrix} J_{(NC)1}(s) \\ J_{(NC)2}(s) \\ J_{(NC)3}(s) \end{pmatrix} \quad (18)$$

where

$$\begin{aligned} Y_{11}(s) &= Y_1(s) + Y_4(s) + Y_5(s) \\ Y_{22}(s) &= Y_2(s) + Y_4(s) + Y_6(s) \\ Y_{33}(s) &= Y_3(s) + Y_5(s) + Y_6(s) \\ Y_{12}(s) &= Y_{21}(s) = -Y_4(s) \\ Y_{13}(s) &= Y_{31}(s) = -Y_5(s) \\ Y_{23}(s) &= Y_{32}(s) = -Y_6(s) \end{aligned} \quad (19)$$

$$
\begin{aligned}
Y_{(c)11}(s) &= Y_{(C)1}(s) + Y_{(C)4}(s) + Y_{(C)5}(s) \\
Y_{(c)22}(s) &= Y_{(C)2}(s) + Y_{(C)4}(s) + Y_{(C)6}(s) \\
Y_{(c)33}(s) &= [Y_{(C)3}(s) + Y_{(C)5}(s) + Y_{(C)6}(s)] \\
Y_{(c)12}(s) &= Y_{(c)21}(s) = -Y_{(c)4}(s) \\
Y_{(c)13}(s) &= Y_{(c)31}(s) = -Y_{(c)4}(s) \\
Y_{(c)23}(s) &= Y_{(c)32}(s) = -Y_{(c)6}(s)
\end{aligned} \qquad (20)
$$

$$
\begin{aligned}
J_{(N)1}(s) &= J_1(s) + J_4(s) - J_5(s) \\
J_{(N)2}(s) &= J_2(s) - J_4(s) - J_6(s) \\
J_{(N)3}(s) &= J_3(s) + J_5(s) + J_6(s)
\end{aligned} \qquad (21)
$$

$$
\begin{aligned}
J_{(NC)1}(s) &= J_{(C)1}(s) + J_{(C)4}(s) - J_{(C)5}(s) \\
J_{(NC)2}(s) &= J_{(C)2}(s) - J_{(C)4}(s) - J_{(C)6}(s) \\
J_{(NC)3}(s) &= J_{(C)3}(s) + J_{(C)5}(s) + J_{(C)6}(s)
\end{aligned} \qquad (22)
$$

$$J_k(s) = E_k(s)Y_k(s) \qquad (23)$$

$$J_{(C)k}(s) = E_k(0)Y_{(C)k}(s) \qquad (24)$$

B. Generalized Matrix Form for Transient Nodal Equation

Equation (18) may be used to generalize new formulated nodal solution of N nodes electrical network in laplace frequency domain as follows

$$
\begin{pmatrix} Y_{11}(s) & Y_{12}(s) & \cdots & Y_{1n}(s) \\ Y_{21}(s) & Y_{22}(s) & \cdots & Y_{2n}(s) \\ \vdots & \vdots & & \vdots \\ Y_{n1}(s) & Y_{n2}(s) & \cdots & Y_{nn}(s) \end{pmatrix} \begin{pmatrix} V_1(s) \\ V_2(s) \\ \vdots \\ V_n(s) \end{pmatrix} - \begin{pmatrix} J_1(s) \\ J_2(s) \\ \vdots \\ J_n(s) \end{pmatrix}
$$

$$
= - \begin{pmatrix} Y_{(C)11}(s) & Y_{(C)12}(s) & \cdots & Y_{(C)1n}(s) \\ Y_{(C)21}(s) & Y_{(C)22}(s) & \cdots & Y_{(C)2n}(s) \\ \vdots & \vdots & & \vdots \\ Y_{(C)n1}(s) & Y_{(C)n2}(s) & \cdots & Y_{(C)nn}(s) \end{pmatrix} \begin{pmatrix} V_{(C)1}(s) \\ V_{(C)2}(s) \\ \vdots \\ V_{(C)n}(s) \end{pmatrix} - \begin{pmatrix} J_{(C)1}(s) \\ J_{(C)2}(s) \\ \vdots \\ J_{(C)n}(s) \end{pmatrix} \qquad (25)
$$

C. Generalized Compact Form For Transient Nodal Equation

For compact form, equation of (23) which is the new s – domain nodal equation by method of complementary circuitry may be written as,

$$\boldsymbol{Y(s)V(s) - J(s) = -\{Y_c(s)V_c(s) - J_c(s)\}} \qquad (26)$$

where

$$
\boldsymbol{Y(s)} = \begin{pmatrix} Y_{11}(s) & Y_{12}(s) & \cdots & Y_{1n}(s) \\ Y_{21}(s) & Y_{22}(s) & \cdots & Y_{2n}(s) \\ \vdots & \vdots & & \vdots \\ Y_{n1}(s) & Y_{n2}(s) & \cdots & Y_{nn}(s) \end{pmatrix} \qquad (27)
$$

Y(s) is laplace frequency domain admittance bus, the admittance bus could be built from fig 2 using any standard method of building an admittance bus so far the branch admittances $Y_k(s)$ of the circuit is evaluated as in equation (10). In this paper it is called the s – domain auxiliary admittance bus

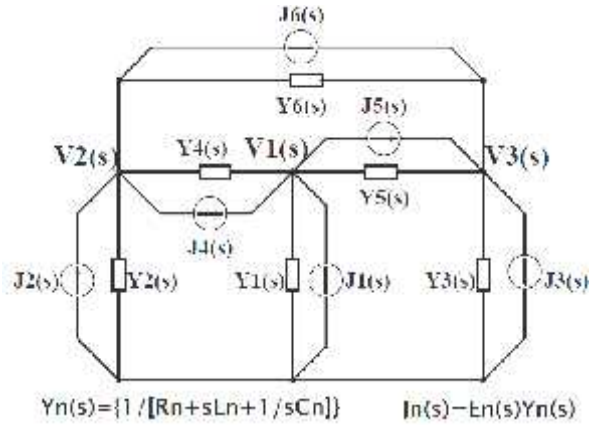

Figure 2: s – domain auxiliary circuit diagram for transient nodal analysis.

Also

$$
\boldsymbol{Y_c(s)} = \begin{pmatrix} Y_{(C)11}(s) & Y_{(C)12}(s) & \cdots & Y_{(C)1n}(s) \\ Y_{(C)21}(s) & Y_{(C)22}(s) & \cdots & Y_{(C)2n}(s) \\ \vdots & \vdots & & \vdots \\ Y_{(C)n1}(s) & Y_{(C)n2}(s) & \cdots & Y_{(C)nn}(s) \end{pmatrix} \qquad (28)
$$

$Y_{(C)}(s)$ is laplace frequency domain dc admittance bus, the admittance bus could be built from fig 3 using any standard method of building an admittance bus when the branch dc admittances $Y_{(C)k}(s)$ of the circuit is evaluated as in equation (9). In this paper it is called the s – domain complementary admittance bus.

also,

$$
\boldsymbol{V(s)} = \begin{pmatrix} V_1(s) \\ V_2(s) \\ \vdots \\ V_n(s) \end{pmatrix}, \qquad \boldsymbol{V_c(s)} = \begin{pmatrix} V_1(0) \\ V_2(0) \\ \vdots \\ V_n(0) \end{pmatrix} \qquad (29)
$$

V(s) is vector of nodal transient voltage in frequency domain, where also $V_{(C)}(s) = V_{(C)}(0)$ and it is the vector of steady state nodal voltages at the instant of transient inception. $V_{(C)}(S)$ is no way transient frequency dependent as indicated by the notation but such configuration is used for uniformity in formula representation, equation (23) and (24).

$$
\boldsymbol{J(s)} = \begin{pmatrix} J_1(s) \\ J_2(s) \\ \vdots \\ J_n(s) \end{pmatrix}, \quad \boldsymbol{J_c(s)} = \begin{pmatrix} J_{(C)1}(s) \\ J_{(C)2}(s) \\ \vdots \\ J_{(C)n}(s) \end{pmatrix} \qquad (30)
$$

J(s) is a vector representing the sum of all the laplace transformed branch source currents incident on the various nodes, while $J_{(C)}(s)$ is a vector representing the sum of all the dc induced transient branch source currents incident on the various complementary circuit nodes fig 3.

where

$$J_k(s) = E_k(s)Y_k(s) \qquad (31)$$

$$J_{(C)k}(s) = E_{(C)k}(0)Y_{(C)k}(s) \qquad (32)$$

$$J_n(s) = \sum_{n=1}^{N} E_n(s) Y_n(s) \quad (33)$$

$$J_{(C)n}(s) = \sum_{n=1}^{N} E_n(0) Y_{(C)n}(s) \quad (34)$$

Definitions

k=1, 2- - - (K – th) branch that are incident on (n – th) node
n=1, 2 - - - (N – th).

$E_k(0)$ → is the (k – th) branch dc value of the source voltage at the instant of transient inception.

$Y_k(s)$ → is the (k – th) branch s - domain transient admittance.

$Y_{(C)k}(s)$ → is the (k – th) branch s - domain complementary admittance due to transient effect on the branch storage element.

$J_k(s)$ → is the (k – th) branch s - domain transient current source.

$J_{(C)k}(s)$ → is the (k – th) branch s - domain complementary transient dc current source.

$J_n(s)$ → is the sum of all the (k – th) branch s - domain transient current source incident on the (n – th) node.

$J_{(C)n}(s)$ → is the sum of all the s - domain (k – th) branch complementary transient dc current source incident on the (n – th) node.

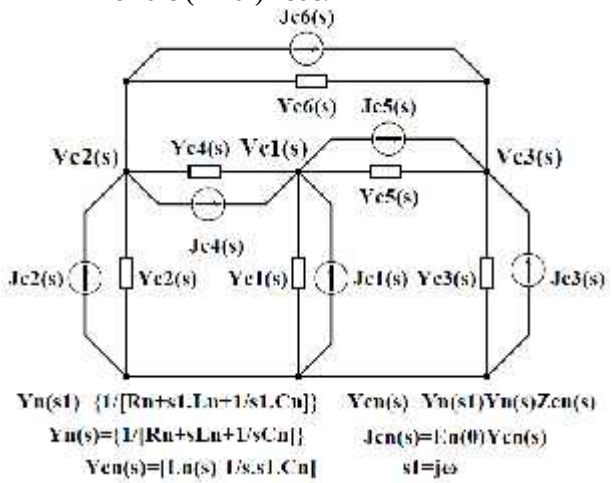

Figure 3: s – domain complementary circuit diagram for transient nodal analysis.

III. ANALYSIS PROCEDURES

1. Solve for the steady state initial nodal voltage, for example

$$YV = J \quad (35)$$

where Y is the steady state admittance bus, V is the steady nodal current source vector, J is the nodal sum current source vector.

2. Convert all the branch elements to laplace equivalent using (10), then transform all the branch voltage sources to laplace equivalent and convert eventually to branch current source using (31).

3. From the branch storage elements formulate the newly derived branch transient dc driving point impedances $Z_{(C)k}(s)$ (12)and from that calculate the branch dc transient driving point admittance $Y_{(C)k}(s)$ (9), then calculate the transient dc current source (32).

Draw the auxiliary laplace admittance diagram as in fig. 2, then build the auxiliary admittance bus (27) by using any of the standard method of steady state admittance bus.

4. From the calculated $Y_{(C)k}(s)$ in step 3, draw the complementary admittance diagram as in fig. 3. From the diagram build the complementary admittance bus (28) as in step 3.

5. From equation (25) solve for V(s) using Cramer's rule

6. Transform V(s) to time domain equivalent using laplace inverse transform. Eg. in Matlab,

$$V(t) = ilap(V(s)) \quad (36)$$

from this nodal voltages could easily be obtained at any instant.

IV. Test Circuit

An earth faulted 100kV - double end fed 100km single transmission line was used for verification of the formulated s – domain transient nodal equation. In this analysis fault position is assumed to be 40%.

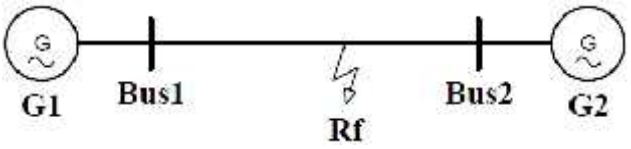

Figure 4: Earth faulted Single line

Test Circuit Parameters
Generator 1
$E1(t)=10x10^4\sin(\omega t)$, $Z_{G1}=(6+j40)\Omega$, S=1MVA
Generator 2
$E2(t)=0.8|E1|\sin(\omega t+45^0)$, $Z_{G2}=(4+j36)\Omega$, S=1MVA
Line Parameters
Rs=0.075 Ω/km, Ls=0.04875 H/km
$Gs=3.75*10^{-8}$ mho/km, $Cs=8.0x10^{-9}$F/km
Line length=100 km, Fault position =40%

V. MODELING

A single pi section was adopted as a model for the test circuit. Normally the model is characterized with constant parameter, shunt capacitance of transmission line is included

in the analysis while shunt conductance is neglected. The equivalent circuit of the test circuit is below fig 5.

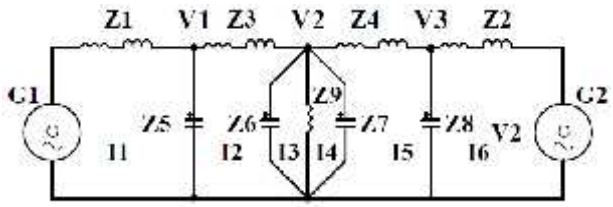

Figure 5: Single line equivalent circuit (PI model) for earth faulted transmission line.

VI. TRANSIENT SIMULATION

A. Symbolic Simulation with Formulated Equation

In this paper the transient nodal voltages were simulated by using the described formulation, the s – domain nodal equation by method of complementary circuitry. Analysis procedures of section 3 were used to calculate the s – domain rational functions of the nodal voltages (29). The obtained s – domain

rational functions were transformed to close form continuous time functions using laplace inverse transformation. Discretization of the close form continuous s - domain functions were done to obtain to plot the nodal voltage response graphs.

B. Simpowersystem Simulation Of Test Circuit

To validate the formulated transient nodal equation, a simulation of the earth faulted line double end fed single transmission were performed using matlab simpowersystem software to obtain the circuit transient nodal voltage responses. Results were compared with the responses obtained from the symbolic simulations using the formulated transient nodal equation.

VII. RESULTS

Nodal voltage response were simulated using the formulated nodal equation and also using simpowersystem package, all simulation were done using Matlab 7.40 mathematical tool. Simulated responses by these methods for the earth faulted double end fed single line transmission were obtained and shown in fig 6 through fig 13. Possible data taking point of node 1and node 3 were taken for various simulating conditions. Simulating conditions included; zero initial condition, non – zero initial condition, high resistive (1000Ω) fault but at zero initial condition, and 1 sec. simulation. All simulations were done, except otherwise stated on 100km line at 40% fault position and 5Ω earth resistive fault. Sampling interval for the formulated equation simulation is 50 μS while that of the simpowersystem simulation is at 5 μS. The over result showed almost 100% conformity between new nodal symbolic formulation and the simpowersystem simulation.

Test Circuit Simulated Nodal Voltage Response Graphs:

100 km Line, 5Ω Resistive Earth Fault with Fault Position at 40% of the line

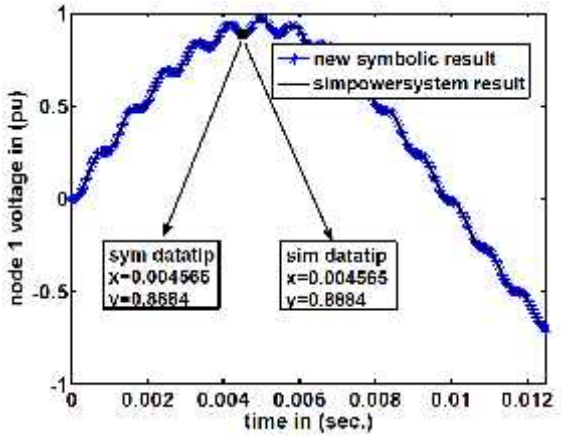

Figure 6: Simulation Of Nodal Voltages Versus Time; 0% Initial Condition.

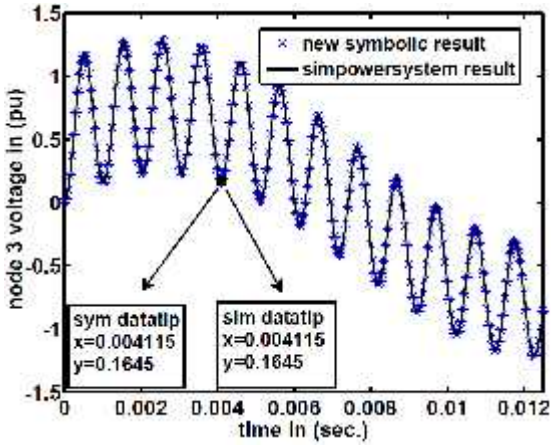

Figure 7: Simulation Of Nodal Voltages Versus Time; 0% Initial Condition.

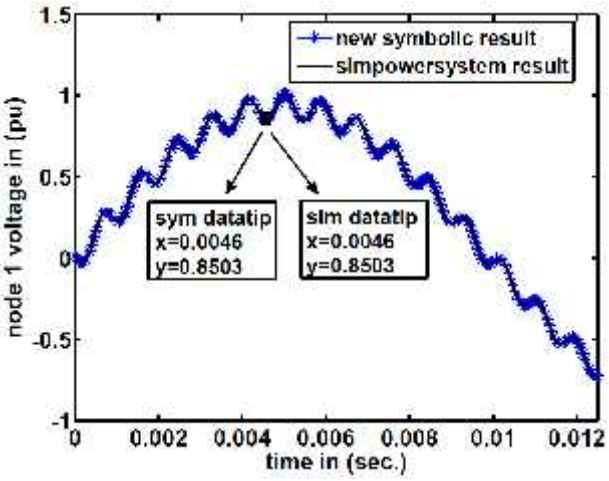

Figure 8: Simulation of Nodal Voltages versus Time; Initial Conditions, 0.15 Sec of Steady State Run.

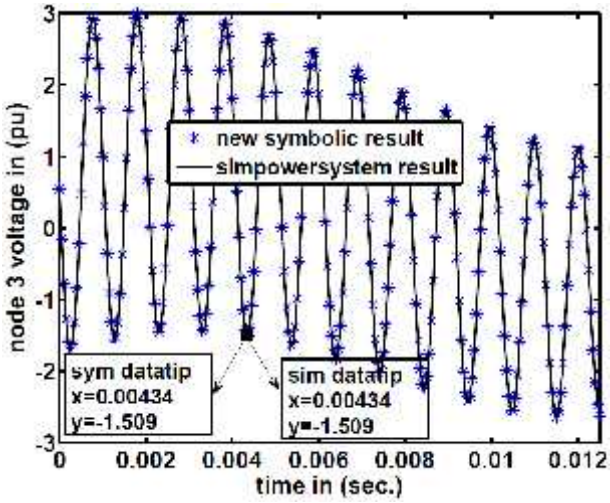

Figure 9: Simulation of Nodal Voltages versus Time; Initial Conditions, 0.15 Sec of Steady State Run.

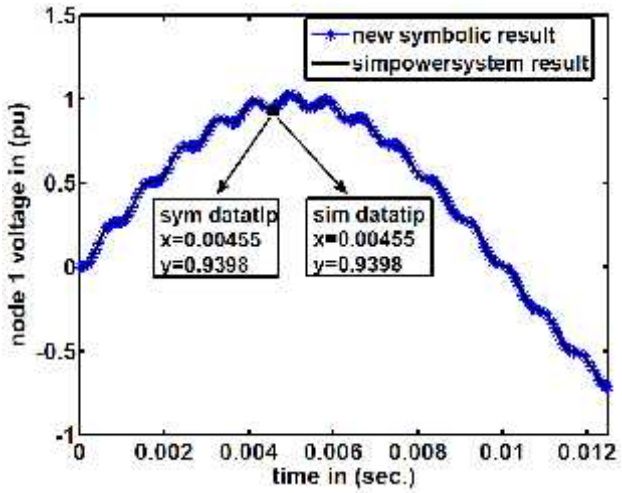

Figure 10: Simulation of Nodal Voltages versus Time; 0% Initial Condition, and 1000Ω Resistive Earth Fault.

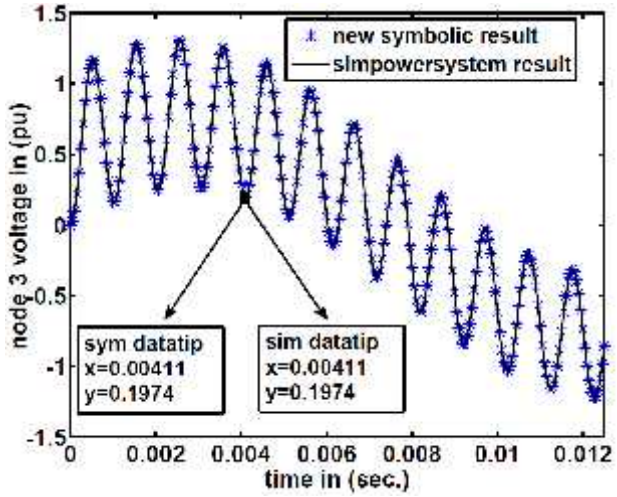

Figure 11: Simulation of Nodal Voltages versus Time; 0% Initial Condition, and 1000Ω Resistive Earth Fault.

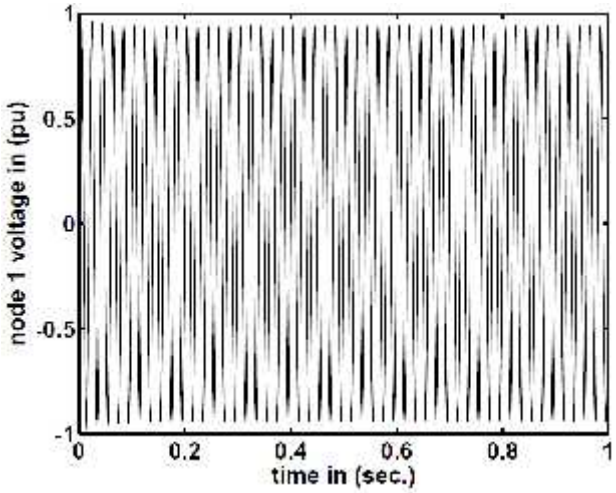

Figure 12: Simulation of Nodal Voltages versus; 0% Initial Condition.

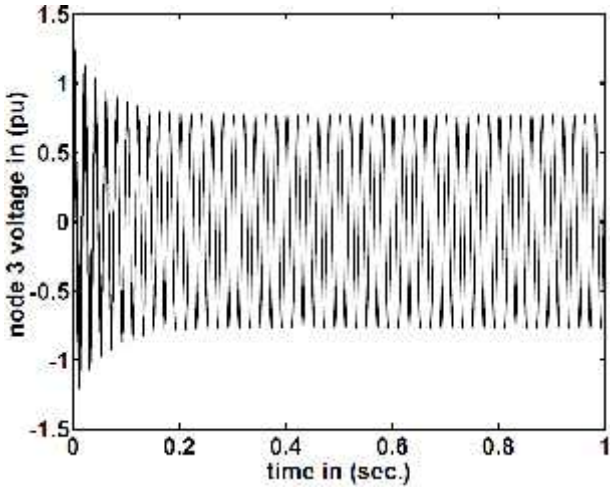

Figure 13: Simulation of Nodal Voltages versus; 0% Initial Condition.

VIII. CONCLUSIONS

Simulation software has been formulated for transient simulation of RLC circuits initiated from steady state. The simulation software is especially useful for power circuits that are modeled with Pi – sections parameter. The result of the simulation of this new symbolic nodal software showed promising conformity with the existing simpowersystem package. The advantage of the new soft is that it is able to simulate complex initial conditions.

IX. REFERENCES

[1] Randal E. Bryant" Symbolic Simulation—Techniques And Applications"

[2] C.-J. Richard Shi And Xiang-Dong Tan "Compact Representation And Efficient Generation of S-Expanded Symbolic Network Functions For computer-Aided Analog Circuit Design" IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 20, No. 7, July 2001

[3] F. V. Fernández, A.Rodríguez-Vázquez, J. L. Huertas, And G. Gielen, "Symbolic Formula Approximation," In Symbolic Analysis Techniques: Applications To Analog Design Automation, Eds. Piscataway, NJ: IEEE, 1998, Ch. 6, Pp. 141–178.

[4] Gielen And W. Sansen, Symbolic Analysis For Automated Design Of Analog Integrated Circuits. Norwell, Ma: Kluwer, 1991.

[5] Mariano Galán, Ignacio García-Vargas, Francisco V. Fernández And Angel Rodríguez-Vázquez "Comparison Of Matroid Intersection Algorithms For Large Circuit Analysis" Proc. Xi Design Of Integrated Circuits And Systems Conf., Pp. 199-204 Sitges (Barcelona), November 1996.

[6] M. Galán, I. García-Vargas, F.V. Fernández And A. Rodríguez-Vázquez "A New Matroid Intersection Algorithm For Symbolic Large Circuit Analysis" Proc. 4th Int. Workshop On Symbolic Methods And Applications To Circuit Design, Leuven (Belgium), October 1996

[7] A. Rodríguez-Vázquez, F.V. Fernández, J.L. Huertas And G. Gielen, "Symbolic Analysis Techniques And

Applicaitons To Analog Design Automation", IEEE Press, 1996.

[8] D. Biolek, V. Biolkov, And J. Dobeš "(Semi) Symbolic Modeling Of Large Linear Systems: Pending Issues"

[9] J.Hsu And C.Sechen, "Dc Small Signal Symbolic Analysis Of Large Analog Integrated Circuits", Ieee Trans. Circuits Syst. I, Vol. 41, Pp. 817–828, Dec. 1994.

[10] W. Chen And G. Shi, "Implementation Of A Symbolic Circuit Simulator For Topological Network Analysis," In Proc. Asia Pacific Conference OnCircuits And Systems (Apccas), Singapore, Dec. 2006.

[11] Z. Kolka, D. Biolek, V. Biolková, M. Horák, Implementation Of Topological Circuit Reduction. In Proc Of Apccas 2010, Malaysia, 2010. Pp. 951-954.

[12] Tan Xd, "Compact Representation And Efficient Generation Of S-Expanded Symbolic Network Functions For Computeraided Analog Circuit Design". IEEE Transaction On Computer-Aided Design Of Integrated Circuits And Systems, 2001. P. 20

[13] Wambacq P, Gielen G, Sansen W, "A New Reliable Approximation Method For Expanded Symbolic Network Functions". IEEE Int. Symposium On Circuits And Systems (Iscas). Atlanta, 1996.

[14] R. Sommer, T. Halfmann, And J. Broz, Automated Behavioral Modeling And Analytical Model-Order Reduction By Application Of Symbolic Circuit Analysis For Multi-Physical Systems, Simulation Modeling Practice And Theory, 16 Pp. 1024–1039. (2008).

[15 Q. Yu And C. Sechen, "A Unified Approach To The Approximate Symbolic Analysis Of Large Analog Integrated Circuits," Ieee Trans. On Circuits And Systems – I: Fundamental Theory And Applications, Vol. 43, No. 8, Pp. 656–669, 1996.

[16] P. Wambacq, R. Fern´Andez, G. E. Gielen, W. Sansen, And A. Rodriguez- V´Zquez, "Efficient Symbolic Computation Of Approximated Small-Signal Characteristics," IEEE J. Solid-State Circuit, Vol. 30, No. 3, Pp. 327–330, 1995.

[17] P. Wambacq, R. Fern´Andez, G. E. Gielen, W. Sansen, And A. Rodriguez- V´Zquez,, "A Family Of Matroid Intersection Algorithms For The Computation Of Approximated Symbolic Network Functions," In Proc. Int'l Symposium On Circuits And Systems, 1996, Pp. 806–809.

[18] O. Guerra, E. Roca, F. V. Fern´Andez, And A. Rodr´Iguez-V´Azquez,, "Approximate Symbolic Analysis Of Hierarchically Decomposed Analog Circuits," Analog Integrated Circuits And Signal Processing, Vol. 31, Pp. 131–145, 2002.

[19] X. Wang and L. Hedrich, An approach to topology synthesis of analog circuits using hierarchical blocks and symbolic analysis, Proc. Asia South Pacific Design Automation Conference, Jan. 2006, pp. 700-705

[20] Ho Cw, Ruehli A, Brennan P (1975). The Modified Nodal Approach To Network Analysis. Ieee Trans. Circuits Syst., P. 22.

[21] Ali Bekir Yildiz "Systematic Generation Of Network Functions For Linear Circuits Using Modified Nodal Approach" Scientific Research And Essays Vol. 6(4), Pp. 698-705, 18 February, 2011

[22] R. Sommer, D. Ammermann, And E. Hennig "More Efficient Algorithms For Symbolic Network Analysis: Supernodes And Reduced Analysis, Analog Integrated Circuits And Signal Processing 3, 73 – 83 (1993)