Circulating Current Produced in a System of Two Inverters Connected in Parallel

Carlos Alonso Sanz, José Miguel Ruiz González, José Antonio Domínguez Vázquez.
Electronics Technology Department. University of Valladolid.
C/Paseo del Cauce, 59. 47011. Valladolid. Spain.

***Abstract*— This paper analyzes the imbalances that produce circulating current in a system of two three-phase Voltage Source Inverters (VSI) with Space Vector Pulse Width Modulation (SVPWM) that, sharing the same DC link, is connected to a balanced three-phase load without galvanic isolation. This analysis has identified two principal imbalances: the difference between the dead times of the two inverters, and the difference between the zero-vector parameters of the two inverters. The first imbalance studied in this paper is generic and can occur in any system of parallel connected inverters. The second imbalance studied in this paper is specific to the space-vector modulation. The study proposes the correction of the imbalances by measurement algorithms and Proportional Integral Control (using the Ziegler Nichols method to tune the controller), in order to reduce or eliminate the circulation current and increase system performance, when the imbalances act independently. It provides a method that does not use an equivalent circuit or a model, determining the value of the imbalance directly and through a system output signal.**

***Keywords*— Inverter, Voltage-Source Inverter (VSI), Space Vector Pulse Width Modulation (SVPWM), Isolated-Gated Bipolar Transistor (IGBT), Circulating Current, Dead-Time, Zero-Vector Parameter, Proportional-Integral (PI), Digital Signal Processor (DSP).**

I. INTRODUCTION

The performance improvement in energy conversion from renewable sources for domestic and industrial uses has focused the efforts of numerous research papers. [1-5]. The parallel connection of inverters allows the most efficient generation profile of each inverter throughout the day to be taken advantage of. The non-isolated connection to the grid or to a load is yet another of the more encouraging points to achieve such an improvement [6-9].

The simplest way to connect inverters in parallel is by using transformers whose outputs are connected together to a load or the electric grid [2]. But this type of connection has such disadvantages as the cost and size of the transformers. It also causes some losses. In order to avoid these drawbacks, the inverters are connected directly, without transformers [21].

When two parallel inverters are attached without galvanic isolation, an internal circulation current may appear [10]. This current means a loss in the system performance, the appearance of DC currents in the inverters and, consequently, a malfunction of the entire system. These phenomena appear when there are differences that cause imbalances between the homologous output voltages of the two inverters [23-31].

II. SYSTEM MODELING

The study has been carried out on a system consisting of two three-phase inverters sharing the same DC input link and connected in parallel to a balanced three-phase resistive load without galvanic isolation, as shown in Fig. 1. The inverters are VSI [2,17], with SVPWM modulation [9,15,21,28,32-33]. It is usually possible to connect different power inverters, so each one can operate at its maximum power performance. In our study, both inverters have the same power performance, and the output voltage of the system is regulated to a constant value.

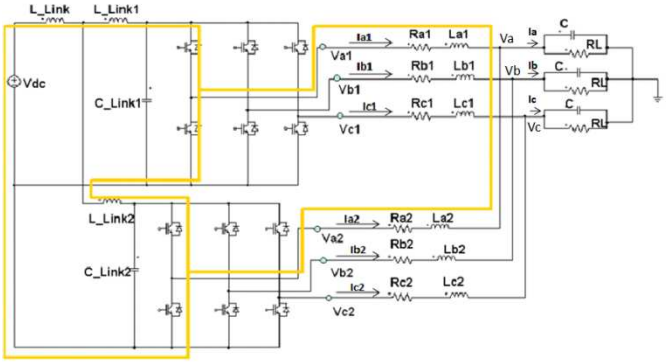


Fig.1 : System formed by two VSI inverters under study with SVPWM modulation.

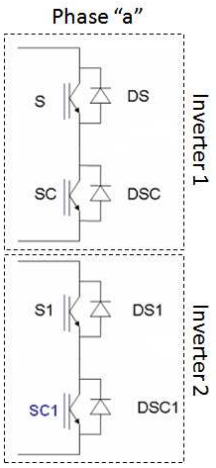


Fig.2 : Representation of IGBTs and antiparallel diodes of the phase "a".

Fig. 2 represents the IGBTs [35-36] and the corresponding antiparallel diodes for the phase "a" of the two inverters shown in Fig. 1. In Table I the characteristic analyzed variables are identified for the circuit of Fig. 1; and in Table II, the values of the magnitudes and the components used in the subsequent experimental analysis are specified.

TABLE I
CHARACTERISTIC ANALYZED VARIABLES IN THE STUDY

Magnitude (unit)	Description
Va1, Vb1, Vc1 (V)	Output voltages of phases "a", "b" and "c" of the inverter 1.
Va2, Vb2, Vc2 (V)	Output voltages of phases "a", "b" and "c" of the inverter 2.
Va, Vb, Vc (V)	Load voltages of the phases "a", "b" and "c"
Ia1, Ib1, Ic1 (A)	Output currents of phases "a", "b" and "c" of the inverter 1.
Ia2, Ib2, Ic2 (A)	Output currents of phases "a", "b" and "c" of the inverter 2.
Ia, Ib, Ic (A)	Load currents of phases "a", "b" and "c".
ICIR (A)	Circulating current of the system
Td1 (µsec)	Dead-time applied to the inverter 1.
Td2 (µsec)	Dead-time applied to the inverter 2.
ΔTd (µsec)	Difference between dead-times (Td1-Td2)
K1	Zero-vector parameter of the inverter 1.
K2	Zero-vector parameter of the inverter 2.
ΔK	Difference between the zero-vector parameters (K1-K2)

TABLE II
VALUES OF THE MAGNITUDES AND COMPONENTS USED IN THE EXPERIMENTAL ANALYSIS

Magnitude	Description	Value (unit)
Vdc	DC-Link	250 V
L_Link	Common Input link inductance of the system	500 µH
L_Link1	Link inductance of the inverter 1.	20 µH
L_Link2	Link inductance of the inverter 2.	20 µH
C_Link1	Link capacitor of the inverter 1.	600 µF
C_Link2	Link capacitor of the inverter 2.	600 µF
Ra1, Rb1, Rc1	Parasitic line resistor for phases "a", "b" and "c" of the inverter 1.	0.5 Ω
Ra2, Rb2, Rc2	Parasitic line resistor for phases "a", "b" and "c" of the inverter 2.	0.5 Ω
La1, Lb1, Lc1	Line inductance for phases "a", "b" and "c" of the inverter 1.	1.0 mH
La2, Lb2, Lc2	Line inductance for phases "a", "b" and "c" of the inverter 2.	1.0 mH
C	Output capacitor phases "a", "b" and "c".	25 µF
RL	Load resistor for phases "a", "b" and "c".	2 Ω
Vce_{SAT}	IGBT collector-emitter saturation voltage	2.5 V
Vth_D	Threshold voltage of the antiparallel diodes	0.7 V
$R_{ON\text{-}IGBT}$	IGBT ON-Resistor	0.1 Ω
$R_{ON\text{-}D}$	Antiparallel diodes ON-Resistor	0.1 Ω
Fs	Carrier frequency	10 KHz
Ts	Period of the carrier component	10^{-4} sec
Fc	Fundamental frequency	50 Hz
Tc	Period of the fundamental component	2 x 10^{-2} sec
V0_reg	RMS output voltage	65 V

III. ORIGIN OF THE CIRCULATING CURRENT

In Fig. 1, one of the paths of phase "a" that connects the output of the inverters with the input DC link is marked. Similarly, it is possible to identify all the paths of the circuit. These paths allow the circulation of internal currents, which supposes power losses in each of the inverters connected in parallel. These currents are defined as "circulating currents" [10,23-29,31]. A difference between the voltages of the homologous outputs is also necessary to produce circulating current inside in the path of the current flow.

In the three-phase system of Fig. 1, the equation defining the circulating current is ICIR (1):

$$ICIR = \frac{(Ia_1 - Ia_2) + (Ib_1 - Ib_2) + (Ic_1 - Ic_2)}{2} \quad (1)$$

There are two ways to eliminate the circulation current. The first is by breaking the return paths, using, for example, transformers (which is not the case of the present study). The second is by eliminating the voltage differences between homologous outputs.

It has been examined two phenomena that cause imbalances between homologous outputs of the inverters, which in turn cause the appearance of circulating currents:

- The difference between the dead-times of the two inverters [11-20,37].
- The difference between the zero-vector parameters of the two inverters [26-28].

The first phenomenon affects every system consisting of two or more parallel connected inverters without galvanic isolation, regardless of the type of modulation used. The second one is specific to the SVPWM modulation. The study proposes methods to monitor and correct imbalances, and also to eliminate the caused circulating current.

IV. EFFECT OF THE DIFFERENCE BETWEEN THE DEAD-TIMES

The non-ideal nature of the power electronic devices, such as the IGBTs and the diodes, the poles of the inverters, need the presence of small delays in the activation of the control signals to prevent short circuits in the input DC link. These time delays applied on the rising edge of the control signals are defined as "dead-times" [11-20,37].

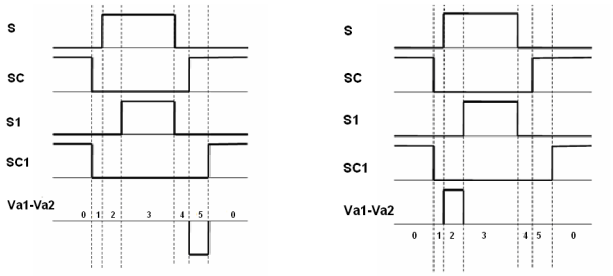
Generally, the difference between the dead-times of the two inverters connected in parallel without galvanic isolation is due mainly to the different power ratings which inverters operate with, so they both have different dead-time references. Even when the two inverters operate at the same nominal power, the lack of synchronization or manufacturing tolerances of the components causes differences in the dead-times of each inverter.

There are many studies and bibliography on the effects of the dead-times on the imbalances and distortions in the output currents for both single-phase and three-phase inverters, working independently or connected to another inverters [12, 14, 16, 18, 19].

The present paper provides a method that does not use an equivalent circuit or a model, and determines how to obtain the value of the current imbalance which causes circulation current directly and through a system output signal.

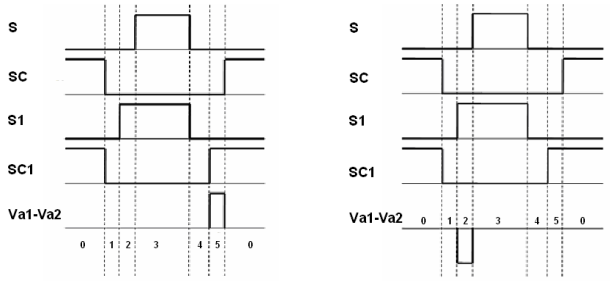
In order to study the system shown in Fig. 1, we suppose it has applied different dead-times, i.e.: Td1≠ Td2. Analyzing one of the phases (phase "a"), and following the diagram of Fig. 2, in Fig. 3, and for the case of Td1<Td2, the activation signals and the difference between the voltages "Va1" and "Va2", when the direction of the

current "Ia" is negative (Fig. 3-a) or positive (Fig. 3-b) has been represented. Similarly, Fig. 4 shows the same signals for the case of Td1>Td2, when the direction of the current "Ia" is negative (Fig. 4-a) or positive (Fig. 4-b). In all figures, six "conduction zones" (numbered from 0 to 5) are identified. Table III identifies the corresponding devices that conduct current through each zone, for the case of Td1<Td2. Table IV identifies the corresponding devices that conduct current through each zone, for the case of Td1>Td2. For Td1< Td2, as for Td1>Td2, (Va1-Va2) are both a square pulse signal whose pulses are repeated "h" times in the period of the fundamental frequency (Ts = 1/Fs).



(a) Negative direction of "Ia" (b) Positive direction of "Ia".

Fig.3 : Activation signal and difference (Va1-Va2) for Td1<Td2.



(a) Negative direction of "Ia" (b) Positive direction of "Ia".

Fig..4 : Activation signal and difference (Va1-Va2) for Td1>Td2.

TABLE III
DEVICES CONDUCTING THROUGH EACH ZONE FOR TD1<TD2

Zone	Negative direction of "Ia"		Positive direction of "Ia"	
	Inverter 1	Inverter 2	Inverter 1	Inverter 2
0	SC	SC1	DSC	DSC1
1	DS	DS1	DSC	DSC1
2	DS	DS1	S	DSC1
3	DS	DS1	S	S1
4	DS	DS1	DSC	DSC1
5	SC	DS1	DSC	DSC1

TABLE IV
DEVICES CONDUCTING THROUGH EACH ZONE FORTD1>TD2

Zone	Negative direction of "Ia"		Positive direction of "Ia"	
	Inverter 1	Inverter 2	Inverter 1	Inverter 2
0	SC	SC1	DSC	DSC1
1	DS	DS1	DSC	DSC1
2	DS	DS1	DSC	S1
3	DS	DS1	S	S1
4	DS	DS1	DSC	DSC1
5	DS	SC1	DSC	DSC1

The pulses have an amplitude equal to "Vdc", so that, in one half cycle, they will have a sign, and, in the other half cycle, they will have the opposite sign. The value "h" is calculated according to (2):

$$h=Fs/Fc \tag{2}$$

The root-mean-square of (Va1-Va2) is (3):

$$\begin{aligned} rms(Va1(t)-Va2(t)) &= \sqrt{\frac{1}{Tc}\int_0^{Tc}[Va1(t)-Va2(t)]^2\,dt} = \\ &= \sqrt{\frac{1}{Tc}\left(\frac{Fs}{Fc}Vdc^2|\Delta Td|\right)} = \\ &= Vdc*\sqrt{Fs*|\Delta Td|} \end{aligned} \tag{3}$$

where ΔTd=(Td1-Td2). Therefore, the value of |ΔTd| is (4):

$$|\Delta Td| = |Td1-Td2| = \frac{[rms(Va1(t)-Va2(t))]^2}{Vdc^2*Fs} \tag{4}$$

That is, if we calculate the RMS value of (Va1-Va2), it is posible to calculate the absolute value of the difference between the dead-times of the two inverters. Regarding the sign of the difference of the dead times, we can observe::

- For Td1<Td2, the first harmonic of "Ia" is always delayed with respect to the first harmonic of the difference of the homologous output voltage.

- For Td1>Td2, the first harmonic of "Ia" is always forwarded with respect to the first harmonic of the difference of the homologous output voltage.

To calculate the sign of ΔTd and for the phase "a", the proposed method analyzes the difference between the first harmonic of "Ia" and the first harmonic of the difference between "Va1" and "Va2". "Ia" is considered to be the reference signal. When "Ia" passes through zero it analyzes, on the one hand, if its slope is positive or negative,and, on the other, if the value of (Va1-Va2) is above or below zero.

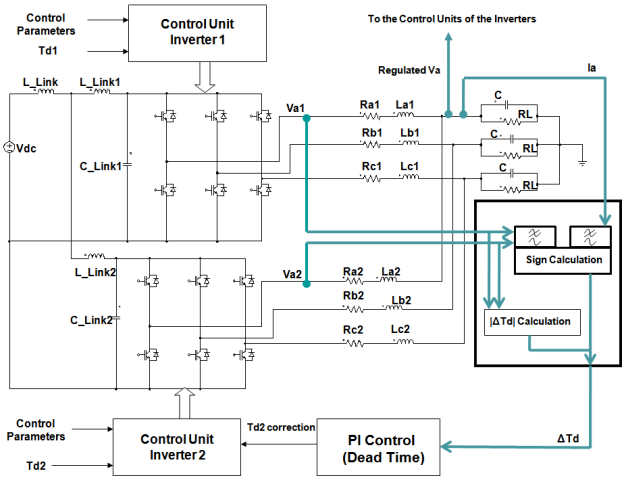


Fig. 5 : Block diagram and proposed control for a difference between of the dead-times of two inverters.

With this information, we can know if "Ia" is delayed or forwarded with reference to the signal (Va1-Va2), and consequently, the sign of ΔTd. Now we know the absolute value and the sign of ΔTd, the PI control is applied [22-23,25,37-38] acting on a module that establishes the dead-time value of the second inverter (Td2). Thus, the difference between the dead-times is eliminated, and consequently the imbalance which causes the appearance of the circulating current is also eliminated. Fig.5 shows the block diagram of the system analyzed.

V. Effect of the Difference Between the Zero-Vector Parameters

When SVPWM modulation is used for generating control signals in a three-phase inverter, it is a common practice to apply a factor or parameter that distributes the width of the zero vectors. This method, defined as "alternating zero-vectors", maintains the properties of the modulation and eliminates disturbances in SVPWM sequence generation. The parameter that allows the sequence of zero-vectors to be distributed is defined as "K" [21-22, 26-28,32-34].

Fig. 6 shows the diagram of control signals for the upper poles of the phases "a", "b" and "c" of an inverter with SVPWM modulation when the parameter "K" is applied.

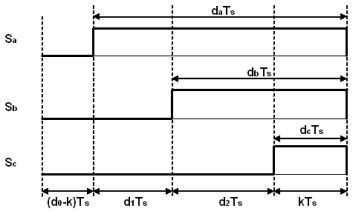


Fig. 6 : Sequence of control signals in the first sector, for an SVPWM inverter on implementing the action of the parameter "K".

The values of the parameters "d_1", "d_2", "d_0" and "k" shown in Fig.6 are defined in (5), (6), (7) and (8).

$$d_1 = M\,\frac{\sqrt{3}}{2}\sin\left(\frac{n\pi}{3}-\theta(t)\right) \tag{5}$$

$$d_2 = M\,\frac{\sqrt{3}}{2}\sin\left(\theta(t)-(n-1)\frac{\pi}{3}\right) \tag{6}$$

$$d_0 = 1-M\,\frac{\sqrt{3}}{2}\left[\sin\left(\frac{n\pi}{3}-\theta(t)\right)+sen\left(\theta(t)-(n-1)\frac{\pi}{3}\right)\right] \tag{7}$$

$$k = K*d_0 = K*\left\{1-M\,\frac{\sqrt{3}}{2}\left[\sin\left(\frac{n\pi}{3}-\theta(t)\right)+sen\left(\theta(t)-(n-1)\frac{\pi}{3}\right)\right]\right\} \tag{8}$$

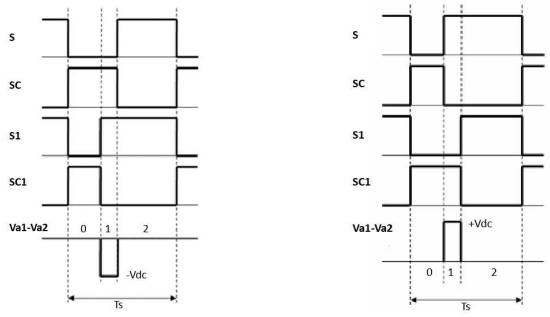
where "K" is the zero-vector parameter (which varies between 0 and 1, and its typical value is 0.5), "n" represents the sector, "θ(t)" the angle that the modulating signal describes, and "M" the modulation index.

In the same way as in the previous case, the difference between the zero-vector parameters of two inverters connected in parallel without galvanic isolation is often due to the different nominal power of each inverter. Even when the two inverters operate at the same power rating, the overall impossible similarity between the two systems results in differences in effective K values of these inverters. There have been many studies on the effects of the zero-vector parameter on the emergence of imbalances and the appearance of internal circulating current phenomena [26-28].

For the circuit of Fig. 1, we suppose that the zero-vector parameter K1 for the inverter 1, and the zero-vector parameter K2 for the inverter 2 are applied, where K1 ≠ K2. Fig. 7 shows the activation signals and the difference voltage (Va1-Va2) for K1<K2 (Fig. 7-a) and for K1>K2 (Fig. 7-b). In these figures, we have identified three "conduction zones" (numbered from 0 to 2). Table V identifies the devices that conduct current for K1<K2, with negative or positive direction of the load current, in each of the zones. Table VI identifies the devices that conduct current for K1>K2, also with negative or positive direction of the load current, in each of the zones. For the case K1<K2, and also for the case K1>K2, the difference of voltages (Va1-Va2) is independent of the direction of the current "Ia", so (Va1-Va2) is a square pulse within the period of the carrier signal, having a width defined in (9):

$$\Delta w = |\Delta K * Ts * d_0| \tag{9}$$

where ΔK = (K1-K2). Therefore, the signal (Va1-Va2) is a pulsed signal.



(a) K1<K2 (b) K1>K2

Fig. 7 : Activation signals and (Va1-Va2) with a difference between the zero-vector parameters of the two inverters.

The pulse height value is named "Vdc" and the width value is directly proportional to the signal d_0 (7), which is not a constant value. However, if the approximation that d_0 is constant and equal to its mean value ($\overline{d_0}$) is performed, we can accept that:

$$\overline{(Va1(t)-Va2(t))} = \frac{1}{Tc}*Vdc*\Delta K*\frac{Tc}{Ts}*Ts*\overline{d_0} = Vdc*\overline{d_0}*\Delta K \tag{10}$$

Therefore, the value of ΔK is (11):

$$\Delta K = \frac{\overline{(Va1(t)-Va2(t))}}{\overline{d_0}*Vdc} \tag{11}$$

With this ΔK definition, and applying the PI control [22-23,25,38], the value of K2 can be corrected and, consequently, we can eliminate the imbalance which causes the appearance of the circulating current. Fig. 8 shows the analyzed circuit, with the applied PI control and the correction system over K2.

TABLE V
DEVICES CONDUCTING FOR EACH ZONE FOR K1<K2

Zone	Negative direction of "Ia"		Positive direction of"Ia"	
	Inversor 1	Inversor 2	Inversor 1	Inversor 2
0	SC	SC1	DSC	DSC1
1	SC	DS1	DSC	S1
2	DS	DS1	S	S1

TABLE VI
DEVICES CONDUCTING FOR EACH ZONE FOR K1>K2

Zone	Negative direction of "Ia"		Positive direction of "Ia"	
	Inversor 1	Inversor 2	Inversor 1	Inversor 2
0	SC	SC1	DSC	DSC1
1	DS	SC1	S	DSC1
2	DS	DS1	S	S1

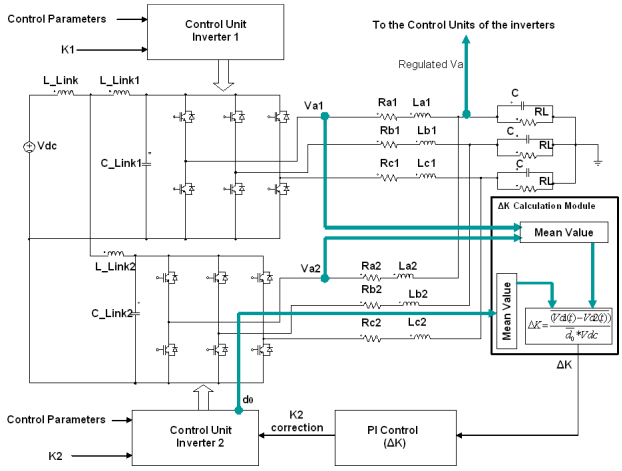


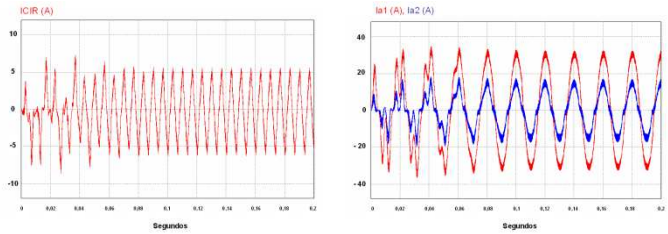
Fig. 8 : Block diagram and proposed control for the imbalance between the zero-vector parameters.

VI. SIMULATION RESULTS

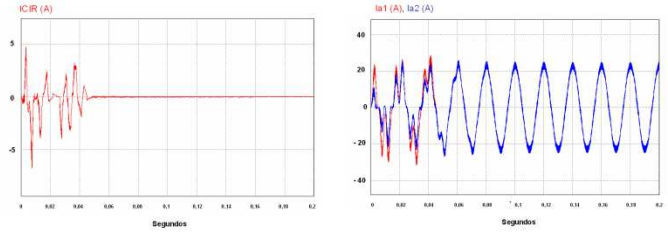
We have performed the simulation using the formulation explained before. The models have been implemented in "PSIM" (Professional Version 9.0.3.400). Considerations included are that both inverters work ideally and simultaneously, and there are not tolerances in the passive components. The imbalances have been introduced in the inverter 2 so control signals have been fed into inverter 2. The output voltage of the system has been regulated ("V0_reg") and, in addition, we use this value as a reference of the SVPWM signal generation of the two inverters. The PI controller tuning has been performed using the Ziegler-Nichols method, verifying the system's stability with the corresponding Bode analysis. The simulation is performed in the sampling period of 1 µsec, with an analysis time horizon of 0.2 sec.

A. Experimental Results for the case "Difference Between Dead-Times".

The results displayed below have been obtained for two different cases: for Td1<Td2 (Fig. 9) and Td1>Td2 (Fig. 10). For the first case, the simulation was performed with Td1=2 µsec and Td2=6 µsec. For the second case, the simulation was performed considering Td1=4 µsec and Td2=2 µsec. Figs. 9-a, 9-b, 10-a, and 10-b show the graphs of "ICIR", "Ia1", and "Ia2", when the system works freely. Figs. 9-c, 9-d, 10-c, and 10-d show the same magnitudes when the proposed control and correction is applied.

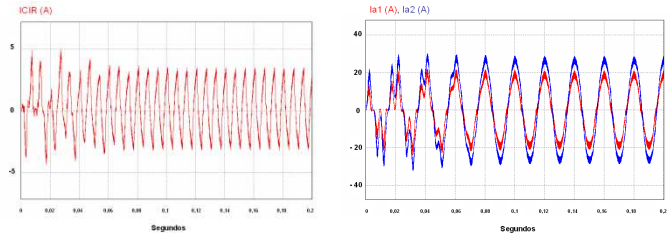


(a) ICIR, without control (b) Ia1 and Ia2, without control

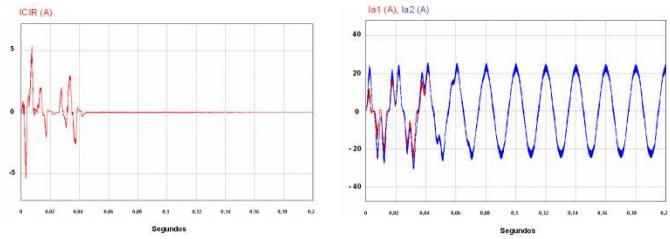


(c) ICIR, with control (d) Ia1 and Ia2, with control

Fig. 9 : "ICIR", "Ia1" and "Ia2" for Td1=2µsec and Td2=6µsec without control (Figs. 9-a and 9-b) and with control (Fig. 9-c and 9-d).



(a) ICIR, without control (b) Ia1 and Ia2, without control



(c) ICIR, with control (d) Ia1 and Ia2, with control

Fig. 10 : "ICIR", "Ia1" and "Ia2" for Td1=4µsec and Td2=2µsec without control (Figs. 10-a and 10-b) and with control (Fig. 10-c and 10-d).

The proposed method is effective and does not require complex calculations. It proposes the calculation of the ΔTd of the system directly, not based on equivalent models. Moreover, it does not require specific external hardware.

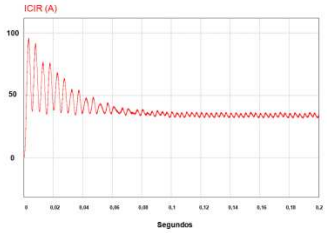
Table VII collects the data input and the output power, and the performance of the system for the two cases analyzed. It should be noted that the reduction of the circulating current increases the system performance. For the first case, in which the initial difference between the dead-times was 4 usec, a performance improvement of 1,94% has been obtained. For the second case, in which the difference between the dead-time was 2 usec, a performance improvement of 0,34% has been obtained.

TABLE VII
POWER VALUES AND PERFORMANCE FOR THE CASES ANALYZED IN SECTION VI.A

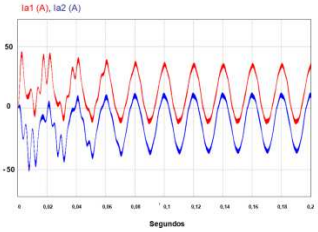
Parameters	Td1=2 µsec, Td2=6 µsec.		Td1=4 µsec, Td2=2 µsec.	
	Without control	With control	Without control	With control
Input Power (W)	7.561	7.388	7.419	7.389
Output Power (W)	6.250	6.250	6.250	6.250
Performance (%)	82,66	84,60	84,24	84,58

B. Experimental Results for the Case of a Difference Between the Zero-Vector Parameters.

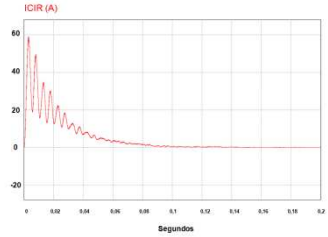
The results displayed below have been obtained for two different cases: for K1>K2 (Fig. 11) and K1<K2 (Fig. 12). Specifically, for the first case, the simulation was performed with K1=0.5 and K2=0.3. For the second case, the simulation was performed for K1=0.5 and K2=0.8. Figs. 11-a, 11-b, 12-a, and 12-b show the graphs of "ICIR", "Ia1", and "Ia2", when the system works freely. Figs. 11-c, 11-d, 12-c, and 12-d show the same magnitudes when applying the proposed control and correction. The method proposed in the present paper obtains the imbalance directly from the system and through the difference of the homologous output voltages of the two inverters, without using an equivalent model. This is a simple method which requires little processing power and obtains controlled signals rapidly.



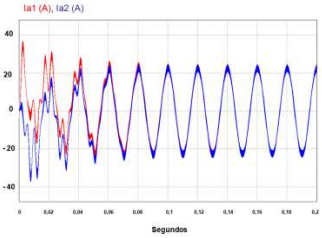
(a) ICIR, without control



(b) Ia1 and Ia2, without control

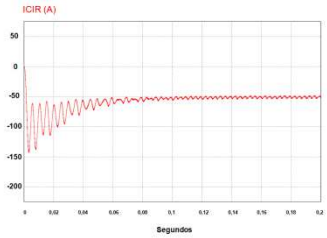


(c) ICIR, with control

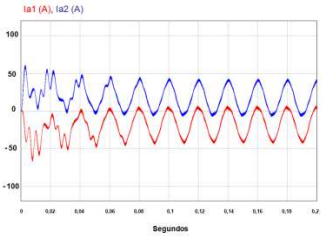


(d) Ia1 and Ia2, with control

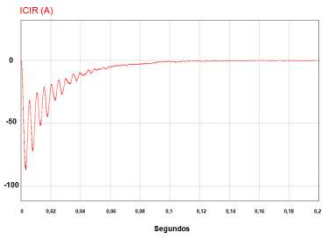
Fig. 11 : "ICIR", "Ia1" and "Ia2" for K1=0.5 and K2=0.3, without control (Figs. 11-a and 11-b) and with control (Fig. 11-c and 11-d).



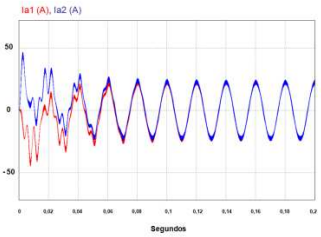
(a) ICIR, without control



(b) Ia1 and Ia2, without control



(c) ICIR, with control



(d) Ia1 and Ia2, with control

Fig. 12 : "ICIR", "Ia1" and "Ia2" for K1=0.5 and K2=0.8, without control (Figs. 12-a and 12-b) and with control (Fig. 12-c and 12-d).

Table VIII collects the data input and the output power, and the performance of the system, for the two cases analyzed. It should be noted that the reduction of the circulating current increases the system performance. For the first case, in which the initial difference between the zero-vector parameters was 0.2, a performance improvement of 5,36 % has been obtained. For the second case, in which the difference between the zero-vector parameters was 0.3, a performance improvement of 10,80 % has been obtained. These enhancement values are very significant because any slight variation between the zero vector parameters of both inverters generates not only harmonic components at multiples of the fundamental frequency, but also continuous components in the output currents and in the circulation current, with non-negligible values. The use of control eliminates them and substantially increases the performance.

TABLE VIII
POWER VALUES AND PERFORMANCE FOR THE CASES ANALYZED IN SECTION VI.B

Parameters	K1=0.5, K2=0.3		K1=0.5, K2=0.8	
	Without control	With control	Without control	With control
Input Power (W)	7.891	7.391	8.470	7.384
Output Power (W)	6.250	6.250	6.250	6.250
Performance (%)	79,20	84,56	73,79	84,59

VII. CONCLUSION

This paper has proposed methods to allow a correction action on one inverter, connected in parallel to another, in order to eliminate the circulation current and thereby increase system performance to the maximum possible value, in case of an imbalance in the dead-times, or in the zero-vector parameters. The proposed procedures are not excessively complex and do not need a high processing capacity. The proposed methods have been validated by quasi-functional simulation, based on a simulator already validated with prototypes of previous inverters.

REFERENCES

[1] F. Schimpf, L. E. Norum, "Grid connected converters for photovoltaic, state of the art, ideas for improvement of transformerless inverters", Nordic workshop on power and industrial electronics, June 9-11, 2008.

[2] B.Soeren, B. Kjaer, J. K. Pedersen, F. Blaabjerg, "A review os single-phase grid-connected inverters for photovoltaics modules", IEEE Transactions on Industry Applications, Vol 41, No 5, Sep 2005.

[3] E.Najafi, A.H.M.Yatim, "Design and implementation of a new multilevel inverter topology", IEEE Transactions on Industrial

Electronics, Vol.: 59 , Issue: 11, pp.: 4148 - 4154, 2012.
[4] G.Petrone, G.Spagnuolo, M.Vitelli, "An analog technique for distributed MPPT PV applications", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 12, pp.: 4713 – 4722, 2012.
[5] O.Lopez-Lapena, M.T. Penella, M. Gasulla, "A closed-loop Maximum power point tracker for subwatt photovoltaic panels", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 3, pp.: 1588 – 1596, 2012.
[6] A. Tuladhar, H. Jin, T. Unger, K. Mauch, "Parallel operation of single phase inverter modules with no control interconnections", Twelfth Annual Applied Power Electronics Conference and Exposition, APEC '97 Conference Proceedings, Vol 1, pp. 94-100, 1997
[7] J.R.Massing, M.Stefanello, H.A.Grundling, H.Pinheiro, "Adaptive current control for grid-connected converters with LCL filter", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 12, pp.: 4681 – 4693, 2012.
[8] H.Xiao, S.Xie, Y.Chen, R.Huang, "An optimized transformerless photovoltaic grid-connected inverter", IEEE Transactions on Industrial Electronics, Vol.58 , Issue: 5, pp.: 1887 – 1895, 2011
[9] Y.A.-R.I. Mohamed, "mitigation of dynamic, unbalanced, and harmonic voltage disturbances using grid-connected inverters with filter", IEEE Transactions on Industrial Electronics, Vol. 58, Issue: 9, pp.: 3914 – 3924, 2011.
[10] T.P. Chen, "Zero-sequence circulating current rduction method for parallel HEPWM inverters between AC bus and DC bus", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 1, pp.: 290 – 300, 2012.
[11] Y. Wang, Q. Gao, X. Cai, "mixed PWM for dead-time elimination and compensation in a grid-tied iInverter", IEEE Transactions on Industrial Electronics, Vol.58, Issue: 10, pp.: 4797 – 4803, 2011.
[12] Z. Guo, F. Kurokawa, "Control and PWM modulation scheme for dead-time compensation of CVCF inverters", Telcommunications Energy Conference, INTELEC 2009. 31st International. 2009, pp.1-6.
[13] J. Kang, G. Xu, C. Zhou, "Study os compensation method on dead-time effects for VSI fed drive systems", in Proc IEEE PESC, pp. 548 - 552, 2007.
[14] H. Zhengyi, J. Xuewu, "A new inverter compensation strategy based on adjusting dead-time on-line", IEEE International Symposium on Industrial Electronics, pp 768-773, 2008.
[15] W. Mao-Gang, Z. Rong-Xian, T. Xin-Zhou, "Dead-time effects analysis and compensation of SPWM an SVPWM", Proceedings of the CSEE, Vol. 26, No 12, pp 101-105, 2006.
[16] Y. Zhang, X. Chen, Y. Kang, J. Chen, "The restrain of the dead-time effects in paralell inverters", IEEE International Conference on Electric Machines and Drives, pp 797-802, 2005.
[17] L. Cheng, F.Z. Peng, "Dead-time elimination for voltage source inverters", IEEE Transaction on Power Electronics, vol 23 No. 2, pp. 574-580, 2008.
[18] G.L.Wang, D.G.Xu, Y. Yu, "A novel strategy of dead-time compensation for PWM voltage-source inverter", Applied Power Electronics Conference and Exposition, 2008, APEC 2008, 23th Annual IEEE, pp. 1779-1783, 2008.
[19] T. Itkonen, J. Luukko, "Switching-function-based simulation model for three-phase voltage source inverter taking dead-time effects into account", 34th Annual Conference of IEEE Industrial Electronics, IECON 2008, pp. 992-997, 2008.
[20] T. Litkonen, J. Luukko, A. Sankala, T. Laakkonen, R. Pollanen, "Modeling and analysis of the dead-time effects in parallel PWM two-level three-phase voltage-source inverters", IEEE Transaction on Power Electronics, Vol 24, Nº 11, pp. 2446-2455, 2009.
[21] C. Tsai, J. Y. Chang, C.M. Lai, Y. L. Juan, Y. H. Liao, "Modeling of circulating current for grid-connected paralell three-phase inverters", SICE Annual Conference, 2008, August 20.22, pp. 1319-1322, 2008.
[22] M.P. Kazmierkowski, L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey", IEEE Transaction on Industrial Electronics, , Vol. 45, No 5, pp. 691-703, 1998.
[23] M. Yu, Y. Kang, Y. Zhang, M. Yin, S. Duan, H. Shan, G. Chen, "A novel decoupled current-sharing scheme based on circulating-impedance in parallel multi-inverter system", 33rd Annual Conference of IEEE Industrial Electronics Society, pp 1668-1672, 2007.
[24] Z. Ye, P.K. Jain, P.C. Sen, "Circulating current minimization in high-frequency AC power distribution architecture with multiple inverter modules operated in parallel", IEEE Transactions on Industrial Electronics, Vol 54, Nº 5, pp 2673-2687, 2007.
[25] L. Chen, L. Xiao, C.Gong, Y. Yan, "Circulating current characteristics analysis and the control strategy of parallel system based on double close loop controlled VSI", IEEE 35th Annual Power Electronics Specialist Conference 2004, Vol 6, pp. 4791-4797, 2004.
[26] Y. Zhang, Z. Jiang, "Zero-sequence current dynamics in parallel-connected voltage source converters", IEEE Electric Ship Technologies Symposium, pp. 189-196, 2009.
[27] Y. Zhang, Z. Jiang, "Sliding mode based zero-sequence current mitigation of parallel-connected power converters", IEEE International Electric Machines and Drives Conference, pp. 1658-1663, 2009.
[28] S. Ji, Y. Yong, Q. Chunqing, "Control of circulating current for direct parallel grid-connected inverters in photovoltaic power generation", International Conference on Mechatronics and Automation, pp. 3805-3810 2009.
[29] Chen, T, "Circulating zero-sequence current control of parallel three-phase inverters", Electric Power Applications, IEEE Proceedings, Vol 153, Issue 2, pp 282-288, 2006.
[30] S. Deshang, D. Kai. G. Zhiquinag, L.Xiaozhong, "Control strategy for input-series–output-parallel high-frequency AC link inverters", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 11, pp.:4101-4111, 2012.
[31] H.Jinwei, W.L.Yun, M.S.Munir, "A flexible harmonic control approach through voltage-controlled DG–grid interfacing converters", IEEE Transactions on Industrial Electronics, Vol.59 , Issue: 1, pp.: 444 – 455, 2012.
[32] S.Hongwu, L.Hua, H. Bi, W. Xingwei, X.A.Limin, "Implementation of voltage-based commutation in space-vector-modulated matrix converter", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 1, pp.: 154-166, 2012.
[33] A.R.Beig, "Synchronized SVPWM algorithm for the overmodulation region of a low switching frequency medium-voltage three-level VSI", IEEE Transactions on Industrial Electronics, Vol 59 , Issue: 12, pp.: 4545 – 4554, 2012.
[34] S.Das, G.Narayanan, "Novel switching sequences for a space-vector-modulated three-level inverter", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 3, pp.: 1477 – 1487, 2012.
[35] R. Kaplar, R. Brock, S. DasGupta, M. Marinella, A. Starbuck,A. Fresquez, S. Gonzalez, J. Granata, M. Quintana, M. Smith, S. Atcitty, "PV inverter performance and reliability: What is the role of the IGBT?", 37th IEEE Photovoltaic Specialists Conference (PVSC), pp. 1842-1847, 2011.
[36] J.Ebrahimi,E.Babaei,G.B.Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components", IEEE Transactions on Industrial Electronics, Vol. 59 , Issue: 2, pp.: 655 – 667, 2012.
[37] N. Hur, K. Nam, S. Won, "A two-degrees-of-freedom current control scheme for dea-dtime compensation", IEEE Transactions on Industrial Electronics,, Vol 47, No. 3, pp. 557-564, 2000.
[38] S. Yang, Q.Lei, F.Z.Peng, Z. Qian, "A robust control scheme for grid-connected voltage-source inverters", IEEE Transactions on Industrial Electronics,Vol. 58 , Issue: 1, pp.: 202 – 212, 2011.