An analytical model for sidewall parasitic capacitance of nano-scale trench isolated MOSFETs

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Abstract— **This paper presents a physics-based, analytical model for sidewall parasitic capacitance of nano-scale MOSFETs. Trench isolated MOSFETs have been considered in the 90 nm technology node. An analytical expression for the trench oxide parasitic capacitance is derived by taking into account the enhanced depletion depth caused due to gate fringing field at the trench oxide sidewalls and dopant redistribution in the channel. The sidewall parasitic capacitance is calculated using conformal mapping technique. The developed model has been validated by comparing the results predicted from the derived model with simulation data and with a similar model available in literature. It has been demonstrated that our model determines more correctly the parasitic capacitance of nano-scale devices compared to the existing model.**

Keywords-nano-scale MOSFETs; shallow trench isolation; inverse narrow width effect; gate fringing field; dopant redistribution; edge effect.

I. INTRODUCTION

For higher packing density and lower power consumption, the present day integrated circuits use narrow transistors. For shallow trench isolated (STI) MOSFETs that are extensively used now, reduction of channel width causes a lowering of the threshold voltage. This is referred to as the inverse narrow width effect (INWE) [1-4]. The existing models available in literature [5-10] had been developed by considering MOS structures of relatively large gate lengths and widths (of the order of few μms) as compared to the state of the art. However, the present day technology demands models for structures in the sub 90 nm regime [11]. This paper presents a physics-based, analytical model for sidewall parasitic capacitance of nano-scale STI MOSFETs. STI MOSFETs have been considered for 90nm technology node. An expression for the sidewall parasitic capacitance along the channel width of the STIMOS device is developed using the conformal mapping technique and by considering the non-uniformity of the depth of the channel depletion layer along the width of the device. The model has been validated by comparing the results predicted from the derived model with those obtained using the device simulator of TCAD Sentaurus [12]. It has been found that the predicted results closely match with the simulation results. The results obtained from our model have also been compared with those obtained from an existing model [4]. The improvement of our model over the existing one has been demonstrated.

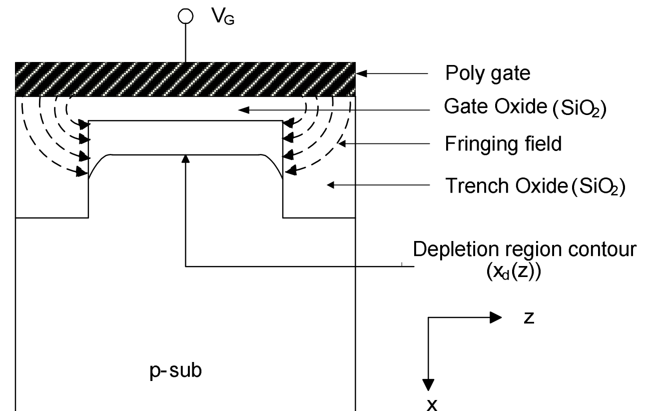

Fig.1 Schematic representation of cross-section along the width of a trench-isolated MOSFET including gate fringing fields.

II. MODEL DERIVATION

A. Physical basis of the model derivation

As the device dimensions scale down, the contribution from the STI edges to the overall channel area increases and starts to dominate the performance [3], [13], [14]. Such impacts arise due to the several physical phenomena.

1) Gate fringing field effect at the STI sidewalls: Figure 1 shows the schematic of the cross-section along the width of the STIMOS device that is used to develop our model.The considerable crowding of the fringing fields through the trench oxide and their termination on the depletion charges under the gate at the sidewall edges causes the surface potential at the sidewall edges to increase in comparison to that at the middle of the channel width. This is referred to as the gate fringing field effect.

2) Dopant redistribution: Dopant redistribution involves two physical phenomena. (i) dopant segregation [15-16] and (ii) transient enhanced diffusion (TED) [17]. Boron segregation reduces the B-concentration near the STI edges. The TED process leads to a substantial decrease of the boron concentration in proximity to the STI edge relative to the centre of the channel. If the device be narrow enough, the decrease in the boron concentration may take place

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significantly even at the centre of the channel.

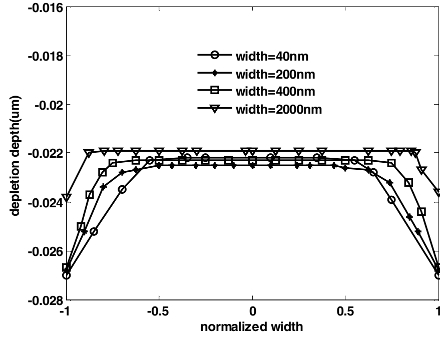

Fig.2. Illustration of edge effect for STI MOSFETs (L=40nm).

3) Non-uniformity of the depletion depth: The enhancement of surface potential at the sidewall edges due to gate fringing field effect results in an increase in the depletion depth at the sidewall edges. The reduced dopant concentration at the sidewalls reinforces the enhanced depletion depth at the trench sidewalls in comparison to that at the middle of the device. Therefore the combined effect of the gate fringing field and dopant redistribution results in an enhanced depletion depth at the sidewall edges. This is referred to as the edge effect. For devices with small widths, the depletion volume near the sidewalls becomes a large percentage of the total depletion volume. The edge effect is illustrated in figure 2. It shows the variation of the depletion depth with the normalized width of five STIMOS devices of length, L=40nm and of different widths. It is observed that as the device becomes narrower, the edge effect increases. The edge effect is conveniently modeled by a sidewall parasitic capacitance in parallel to the gate oxide capacitance [5]. Thus, the total gate capacitance constitutes the gate oxide capacitance in parallel with two sidewall parasitic capacitances.

B. Determination of sidewall parasitic capacitance:

The total gate capacitance of an STIMOS device is written as [18]

$$C_g = C_{ox}WL + 2C_{STI} \tag{1}$$

where, C_{ox} is the oxide capacitance per unit area, W is the channel width, L is the channel length and C_{STI} is the parasitic capacitance.

$$C_{STI} = C_P \times L \tag{2}$$

C_P is the parasitic capacitance per unit length of the STIMOS device. In order to determine the parasitic capacitance C_P, let us first consider a typical variation of the depletion depth along the width of the device as shown in Fig. 3(a). In this figure, $W =$ device width, $d_W = x_d\left(W/2\right) =$ depletion depth in the middle of the device measured from the top semiconductor- oxide interface to the bulk of the

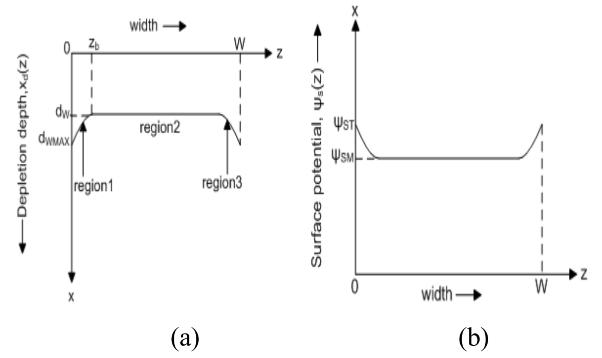

Fig.3 (a) Variation of depletion depth along the channel width. (b) Variation of surface potential along the channel width.

semi-conductor. $d_{WMAX} = x_d(0) = x_d(W) =$ depletion depth at the sidewalls. As shown in Fig. 3(a), the depletion depth profile can be divided into three regions. In the first region, the depletion depth at the oxide sidewall, as measured from the semiconductor-oxide interface is $d_{w\max}$ which then gradually decreases to d_w. Beyond a critical point z_b, the depletion depth remains constant at d_w in the second region and finally increases again to $d_{w\max}$ in the third region. Fig. 3(b) shows the variation of the surface potential along the width of the device. The gate fringing field through the trench oxide causes the surface potential at the sidewall edges to increase in comparison to that at the middle of the channel width. From Fig. 3(b) the following quantities are defined. $\psi_{SM} = \psi_s\left(W/2\right) =$ surface potential at the mid-width of the device. $\psi_{ST} = \psi_s(0) = \psi_s(W) =$ surface potential at the trench oxide sidewall edges. The electrostatic potential decreases quadratically along the two sidewalls in the depletion region. Accordingly, this variation is taken as:

$$\psi = \psi_{ST}\left(1 - \frac{x}{d_{WMAX}}\right)^2; \quad 0 \le x \le d_{WMAX} \tag{3}$$

Here, $$d_{WMAX} = \sqrt{\frac{2\varepsilon_{si}}{qN_a}}\sqrt{\psi_{ST}} \tag{4}$$

where, ε_{si} is the permittivity of silicon, N_t is the doping concentration at the trench oxide sidewall. The two-dimensional electrostatic potential distribution at any point in the depletion region of the semiconductor is obtained by solving Poisson's integral formula and using conformal mapping technique as

$$\phi(x,z) = \frac{\psi_{ST}}{\pi}\left[\begin{array}{l}\left(2xz\left(x^2 - z^2 - d_{WMAX}^2\right)\right)\ln\left(\dfrac{4x^2z^2 + \left(x^2 - z^2 - d_{WMAX}^2\right)^2}{4x^2z^2 + \left(x^2 - z^2\right)^2}\right) + 2d_{WMAX}^2 xz - \\ \left(\left(x^2 - z^2 - d_{WMAX}^2\right)^2 - 4x^2z^2\right)\left(\tan^{-1}\left(\dfrac{x^2 - z^2 - d_{WMAX}^2}{2xz}\right) - \tan^{-1}\left(\dfrac{x^2 - z^2}{2xz}\right)\right)\end{array}\right] \tag{5}$$

$/ d_{WMAX}^4$

The charge associated along the sidewall is then derived as

$$Q = \varepsilon_{ox} \int_{0}^{d_{WMAX}} -\left(\frac{\partial \phi}{\partial z}\right)\bigg|_{z=0} dx \tag{6}$$

$$= \frac{\varepsilon_{ox}\psi_{ST}}{\pi} F \tag{7}$$

where,

$$F = \left[-\ln\left(\frac{d_{WMAX}^2}{x^2} - 1\right) \; 1 - \frac{x^2}{d_{WMAX}^2} \;^{2} - \frac{x^2}{d_{WMAX}^2} \right]\Bigg|_{x_{lower}}^{x_{upper}} \tag{8}$$

Here, $x_{upper} = d_{WMAX}$ and $x_{lower} = 0$, ideally. However, to have mathematical solution, we take x_{upper} to be a value very close to d_{WMAX} and x_{lower} to be a value very close to 0. We observe from equation (7) that in order to determine the sidewall charge we need to determine the surface potential at the trench-oxide sidewall, i.e., ψ_{ST} .

1) Determination of sidewall surface potential, ψ_{ST} : As obtained from simulation results, Both ψ_{SM} and ψ_{ST} vary with V_{GS} linearly in the weak inversion region (Fig. 4). Therefore, we argue that the quantities ψ_{SM} and ψ_{ST} , in the weak inversion region, are related to each other by a simple linear relation. Simulation results showing the variation of ψ_{SM} and ψ_{ST} in the weak inversion region, (shown in Fig. 5) support this argument. Accordingly, ψ_{ST} is expressed as

$$\psi_{ST} = l\psi_{SM} + d \tag{9}$$

where, l is close to unity and d is a numerical constant which is expressed as $d = \frac{nkT}{q}$ where, $\frac{kT}{q}$ is the volt equivalent of temperature and n is an empirically fitted parameter used to provide reasonable results. The value of n has been found to lie between 1.2 and 2.3 for devices with largely varying dimensions like 200nm gate length to 40nm gate length having substrate doping ranging from 1e+17/cc to 1e+19/cc. The surface potential in the middle of the channel width for a nano-scale device, i.e., ψ_{SM} is written as

$$\psi_{SM} = \left(-\frac{\alpha_L \gamma}{2} + \sqrt{\frac{{\alpha_L}^2 \gamma^2}{4} + \left(V_{GB} - V_{FB}\right)} \right)^2 \tag{10}$$

Here, $\gamma = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}^{'}}$ is the back-gate factor and the factor α_L incorporates the effect of short channel length of the device.

All the other notations signify their standard meanings. It is clear from (9) and (10) that ψ_{ST} is a function of the gate bias V_{GB} . Thus equation (7) is written as

$$Q = \frac{\varepsilon_{ox}}{\pi} F f(V_{GB}) \tag{11}$$

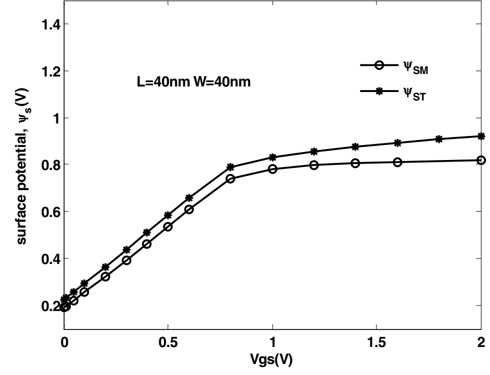

Fig. 4 Simulation Results showing variation of ψ_{ST} and ψ_{SM} with V_{GS} (V_{SB} =0V).

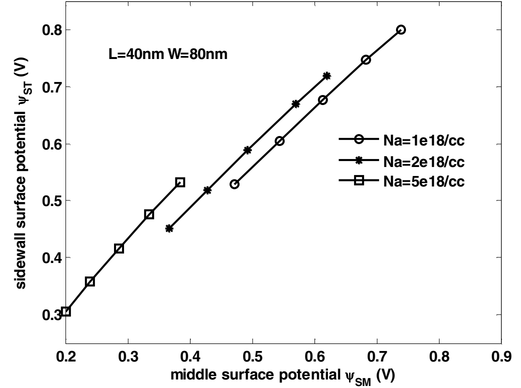

Fig. 5 Plot of ψ_{ST} versus ψ_{SM} for different substrate concentrations.

or,

$$Q = C_P f(V_{GB}) \tag{12}$$

where, C_P is the parasitic capacitance per unit length and is written as

$$C_P = \frac{\varepsilon_{ox}}{\pi} F \tag{13}$$

Using C_F from (8) and (13), C_{STI} is calculated from (2) as

$$C_{STI} = \frac{\varepsilon_{ox}}{\pi} L \left[-\ln\left(\frac{d_{WMAX}^2}{x^2} - 1\right) \; 1 - \frac{x^2}{d_{WMAX}^2} \;^{2} - \frac{x^2}{d_{WMAX}^2} \right]\Bigg|_{x_{lower}}^{x_{upper}} \tag{14}$$

III. Results and Discussions

We have considered an STI MOS structure as shown in Fig. 6. The chosen technology parameters are based upon the International Technology Roadmap [11]. Figure 7 shows plots of the electrostatic potential along the sidewall versus depth of a typical STIMOS device. It shows results as obtained from our model (equation (3)) which are then compared with those obtained from the TCAD Sentaurus device simulator and with those obtained from an existing work [6]. We observe that the results predicted from our model are in more close agreement

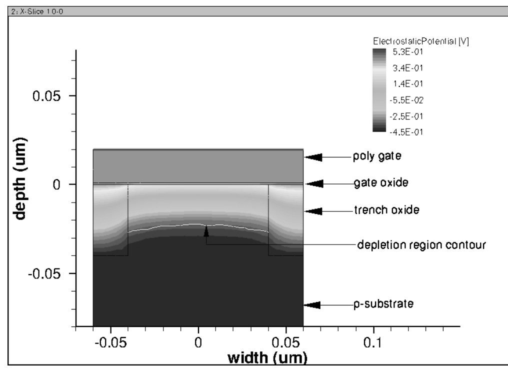

Fig. 6 Cross section along the width of a trench-isolated MOSFET as obtained from the device simulator.

to the simulation results. Figure 8 shows the plots of the total gate capacitance normalized to the gate oxide capacitance against the width of the device. It indicates a capacitance increase of upto 18% for small gate widths. The corresponding results obtained from model in [4] have also been plotted. The model in [4] shows the increase by only about 10%. This confirms the underestimation of the gate capacitance by the earlier model in [4].

IV. CONCLUSION

In this paper, an analytical model for sidewall parasitic capacitance of nano-scale STI MOSFETs has been developed in the 90 nm technology node. The parasitic capacitance along the width of the device was evaluated using conformal mapping technique. The model takes into account the enhanced depletion depth at the trench oxide sidewalls due to edge effect caused by gate fringing and dopant redistribution. The device parameters have been chosen according to the ITRS specifications. The developed model has been validated by comparing the results predicted from the derived model with results obtained from the device simulator of TCAD Sentaurus. The performances of the derived model have also been compared with those of a standard model available in literature.

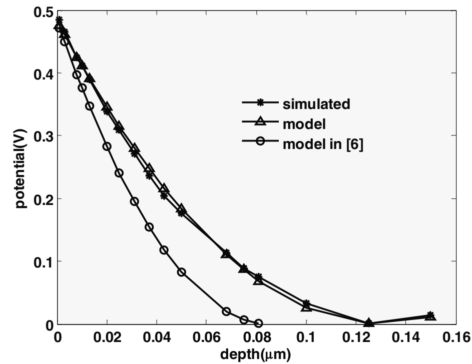

Fig. 7 Electrostatic potential versus depth along the sidewall.

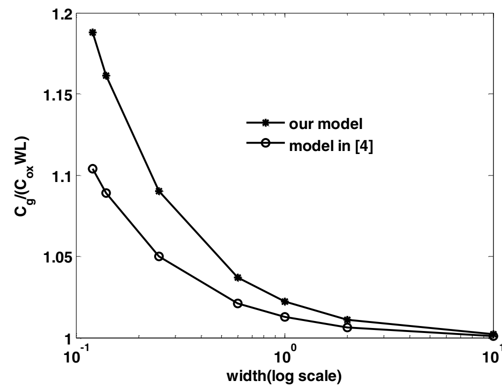

Fig. 8 Total gate capacitance normalized to the gate oxide capacitance against the width of the device.

REFERENCES

[1] Lau W.S et al., “Anomalous narrow width effect in p-channel metal-oxide-semiconductor surface channel transistors using shallow trench isolation technology”, Microelectronics Reliability, vol.48, pp. 919-922, Jun. 2008.

[2] Xinfu L. et al., “A study of inverse narrow width effect of 65nm low power CMOS technology”, IC SICT, pp. 1138-1141, 2008.

[3] Wang RV., Lee YH., Lu YL R., McMahon W., Hu S., Ghetti A., “ Shallow trench isolation edge effect on random telegraph signal noise and implications for flash memory”, IEEE Trans. Electron Devices, vol. 56, no.9, pp. 2107-2113, Sept., 2009.

[4] Pacha C., Martin B., von Arnim K., Brederlow R., Schmitt-Landsiedel D., Seegebrecht P., Berthold J., Thewes R., “Impact of STI-induced stress, inverse narrow width effect, and statistical VTH variations on leakage currents in 120 nm CMOS”, ESSDERC, pp., 397-400, 2004.

[5] L.A.Akers, “The inverse narrow width effect”, IEEE Electron Device Lett, vol. EDL-7, pp. 419-421, July 1986.

[6] Hong K.M and Cheng Y.C, “An analytical model for the inverse narrow-gate effect of a metal-oxide-semiconductor field-effect transistor”, J. Appl. Phys., vol. 61, pp. 2387–2392, Mar. 1987.

[7] Hsueh K.K.L, Sanchez J.J, Demassa T.A and Akers L.A, “Inverse-Narrow-Width Effects and Small-Geometry MOSFET Threshold Voltage Model”, IEEE Trans. Electron Devices, vol. 35, no.3, pp. 325-338, Mar. 1988.

[8] Agrawal B, De V.K and Meindl J.D, “Three-Dimensional Analytical Subthreshold Models for Bulk MOSFETs”, IEEE Trans. Electron Devices, vol. 42, no.12, pp. 2170-2180, Dec. 1995.

[9] Noor A and Shekhar C, “3D Analytical Model for Threshold Voltage of Small-Geometry MOSFET”, Solid-State Electronics vol. 39, no. 5, pp. 745-751, 1996.

[10] Lin S.C, Kuo J.B, Huang K.T, and Sun S.W, “A Closed-Form Back-Gate-Bias Related Inverse Narrow-Channel Effect Model for Deep-Submicron VLSI CMOS Devices Using Shallow Trench Isolation” IEEE Trans. Electron Devices, vol. 47, no. 4, pp. 725-733, Apr. 2000.

[11] International Technology Roadmap for Semiconductors, 2007.

[12] TCAD Sentaurus Manuals, Version Y-2006.06, Synopsys Inc.

[13] Li Zhiguo, Yang F, Wang J, Lin P, Chang J, Wang Y, Yi C, and Yan F, “The Impact of Shallow Trench Isolation on the Channel Hot Electron Programming Behaviors of SONOS Cells”, ECS Transactions, pp 43-48, 2009.

[14] Sheu Y M, Yang S J, Wang C C, Chang C S, Huang L P, Huang T Y, Chen M J, and Diaz C H, “Modeling Mechanical Stress Effect on Dopant Diffusion in Scaled MOSFETs”, IEEE Trans. Electron Devices, vol. 52, no. 1, pp. 30-38, Jan. 2005.

[15] Arnaud F, Bidaud M, “Gate Oxide Process Impact on RNCE for Advanced CMOS Transistors”, ESSDERC 2002.

[16] Nouri F, Scott G, Rubin M and Manley M, “Narrow Device Issues in Deep-Submicron Technologies-the Influence of Stress, TED and Segregation on Device Performance”, Proceedings of ESSDERC 2000, pp. 112-115.

[17] Ghetti A, Benvenuti A, Molteni G, Albenci S, Soncini V and Pavan A, “Experimental and Simulation Study of Boron Segregation and Diffusion during Gate Oxidation and Spike Annealing’, IEDM, pp. 983-986, 2004.

[18] Tsividis Y.P, “Operation and Modeling of the MOS Transistor”, 2nd Ed. New York: McGraw-Hill, 1999.