Noise Performance of Gate Engineered Double Gate MOSFETs for Analog and RF applications

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***Abstract*—Due to their excellent scalability and better immunity to short channel effects, Double gate MOSFETs rule the CMOS applications era. However for channel lengths below 100nm, DG MOSFETs still show considerable threshold voltage roll off and to overcome this, gate engineering technique can be widely used. In this paper, we systematically investigate the analog/RF and Noise performance of Gate engineered DG MOSFETs for System-on-chip applications. A very good improvement in noise parameters such as power spectral density and Noise figure are observed in case of DMDG devices compared to its single metal counterpart.**

Keywords-Dual-metal double gate (DM-DG), radio-frequency (RF) applications, Noisefigure, power spectral density and cut-off frequency.

I. INTRODUCTION

The use of low power, low noise devices for future electronic applications is becoming more and more important. Especially, SOI devices are excellent candidates to become an alternative for conventional bulk CMOS. Advanced MOSFET structures such as ultrathin-body silicon-on-insulator (SOI) and the double-gate (DG) can be scaled more aggressively than the bulk-Si structures and hence may be adapted for IC production. A fully depleted double-gate SOI offers a higher drive current than its single-gate (SG) counterpart due to larger control over the channel region, and this strongly enhances the immunity towards the short channel effects (SCEs) and provides almost ideal sub-threshold slopes. Metallic gate electrodes is necessary for these devices to provide maximum performance benefit over bulk-Si MOSFETs. The influence of both channel and gate engineering on the analog and RF performances of double-gate (DG) MOSFETs for system-on-chip applications are studied[1-2]. The gate engineering technique used here is the dual-metal gate technology, and channel engineering technique is the conventional doping process. For analog applications, importance is given to the subthreshold regime as CMOS circuits operated in this regime are very much attractive for ultralow-power high-gain performances[3-6].

In this work, we have systematically investigated the analog performances as well as the RF parameters for high frequency applications of n-channel advanced CMOS devices with 100nm gate length. The Dual Metal Gate realized on the double gate architecture has been investigated. Integrated Systems Engineering (ISE) - Technology Computer-Aided Design (TCAD) has been used for the realization and the analysis of all the devices used in this study. All the device parameters are set as per ITRS road map for the 100nm gate length.

Once we decide the fabrication process of our chip, the amount of intrinsic device noise is fixed. Modeling can provide the understanding of this intrinsic noise and aid in design optimization of circuits. Due to the randomness of noise, we need to use statistical approaches for its characterization. Generally, the average of noise current is zero; hence the power spectral density of noise per unit frequency is used for the expression of noise. Noise figure and power spectral density are the two main parameters that describes the amount of noise in an electronic device[7].

II.DEVICE STRUCTURE AND SIMULATION

The technology parameters and the supply voltages used for device simulations are according to the International Technology Roadmap for Semiconductors for 100-nm gate-length devices. The two structures under consideration have an oxide thickness of 3nm and a silicon film thickness of 30nm. The devices are optimized to make a successful comparison of different RF and Noise parameters. . In DG, the silicon film is kept practically undoped (10^{15} cm^{-3}) and the gate work function of single gate material is fixed at 4.577eV to obtain the threshold voltage of 0.3V at a drain voltage of 0.1V. The schematic cross-sectional view of an n-channel DG MOSFET with DMG technology is shown in Fig.1. The optimization of

DMG technology is done by choosing metals M1 (molybdenum) and M2(aluminium) whose workfunctions are 4.55 and 4.1 eV respectively. The metals have equal lengths and device produce a threshold voltage of 0.3V at a drain voltage of 0.1V.

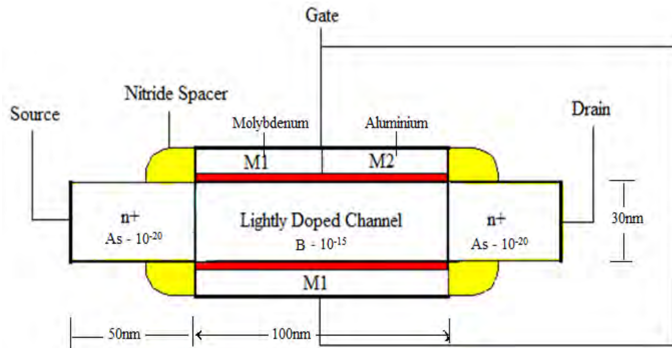

Fig.1. Cross sectional view of DM-DG MOSFET

A systematic comparison is carried out between the conventional DG MOSFET and the gate engineered DG MOSFET (DM-DG) for analog & RF applications. The Electrostatic surface potential along the channel for DG and DM-DG n-channel MOSFETs for drain voltages of 2.0V and gate voltage of 1.0V is shown in Fig.2. In this figure, the position along the channel is plotted in X-axis direction, where "0" indicates the centre of the channel. The DM-DG device shows a step potential profile at the interface of the two metals along the channel. It is clearly visible that the DM-DG technology provides a larger increase of potential, so that the major portion of the channel is shielded from the drain voltage variations compared with other device, thereby improving DIBL characteristics. It is seen that for DM-DG MOS devices, the electric field discontinuity at the interface of two gate metals causes channel field flattening which results in larger average velocity when the electrons enter the channel from the source.

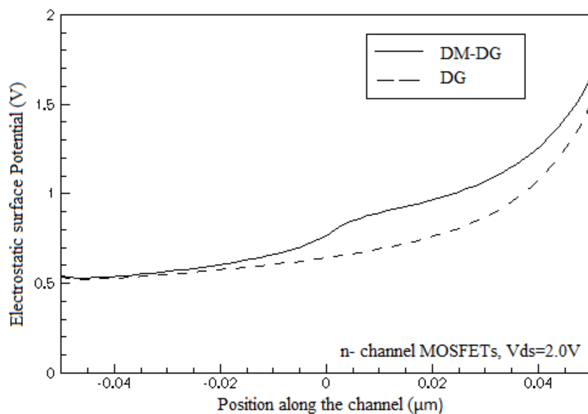

Fig.2. Comparison of electrostatic surface potential for n-channel DM-DG and conventional DG MOSFETs for a drain voltage of V_{ds}=2.0V

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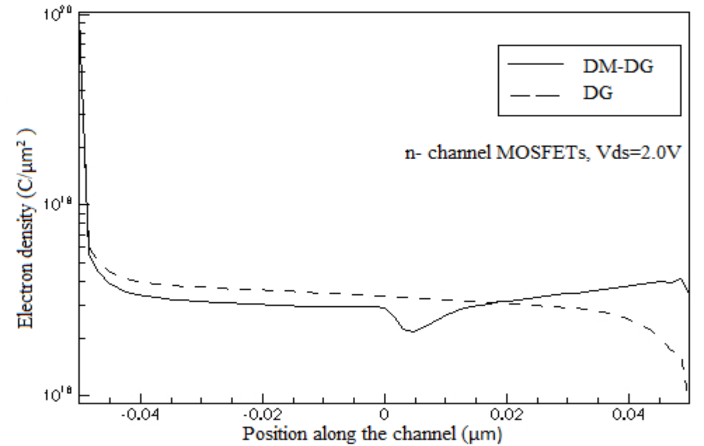

Fig.3: Comparison of Electron density of n-channel DG and DM-DG MOSFETs for a V_{ds} = 2.0V

The electron density along the channel length for DG and DM-DG n-channel MOSFETs for a drain to source voltage, V_{ds} = 2.0V is shown in the Fig.3.

The electron density of the conventional DG MOSFET is almost saturated whereas there is a discontinuity in the electron density at the interface of two metals for DMDG MOSFETs. This effect provides immunity to device towards SCEs.

III. Result and Discussion

A. Analog-RF performance

The important analog performance parameter transconductance g_m is observed for a gate voltage of 2.0V is shown in Fig. 4. The proposed DM-DG device shows improved transconductance by 7 %.

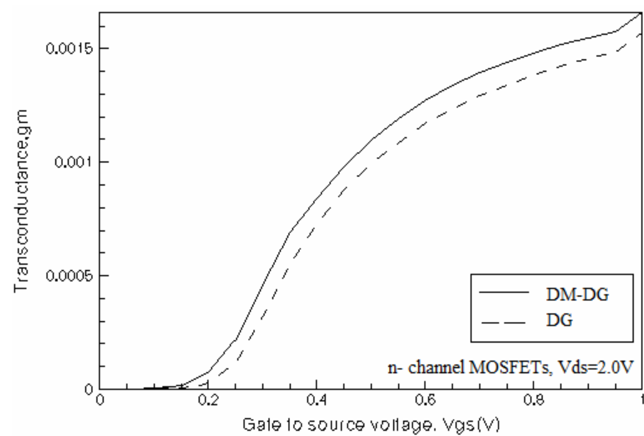

Fig.4.: Comparison of the Transconductance for n-channel DG and DM-DG MOSFETs as a function of gate-to-source voltage for V_{ds} = 2.0V

The cutoff frequency f_T and the gain bandwidth f_A are the two important parameters for evaluating the device potentials for RF

applications. The cutoff frequency f_T is the frequency when the current gain is unity. The approximate values of f_T and f_A are given in the following equations,

$$f_T \approx \frac{g_m}{2.\pi.C_{gs}} \quad (1)$$

$$f_A \approx \frac{g_m}{2.\pi.10.C_{gd}} \quad (2)$$

where C_{gs} is gate-to-source capacitances, C_{gd} is gate-to-drain capacitance and g_m is the transconductance. In 2-D device simulator, AC analysis is performed and Y-parameters are computed. All capacitances are extracted from the small signal ac device simulations at a frequency of 1MHz.The electron density at the source end is considerably less compared to that at the drain end in the case of the DM-DG device. This is due to the fact that the channel at the source side has a higher threshold voltage due to the higher work function material at source side.

The resulting cutoff frequency and gain bandwidth which depends on the ratio of transconductance and gate capacitance is higher for the DM-DG device, as shown in Fig.5 and Fig. 6 respectively.

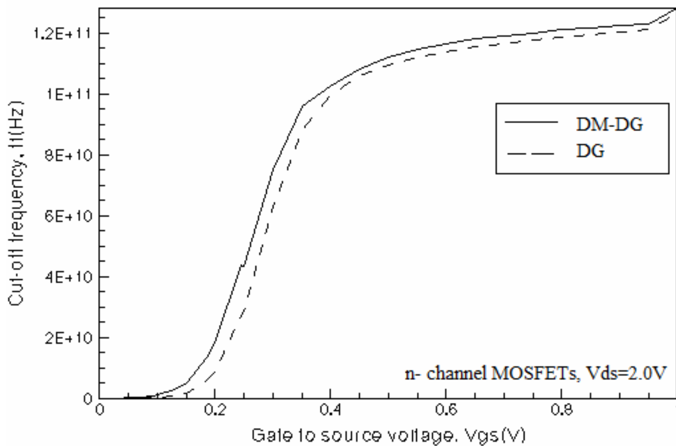

Fig.5: Comparison of the cutoff frequency for n-channel DG and DM-DG MOSFETs as a function of gate-to-source voltage for V_{ds} = 2.0V

From Fig.6, it is evident that the DM-DG devices show improved gain bandwidth due to increased transconductance (g_m). Improved transconductance makes the DM-DG device better for analog System-on-chip applications.

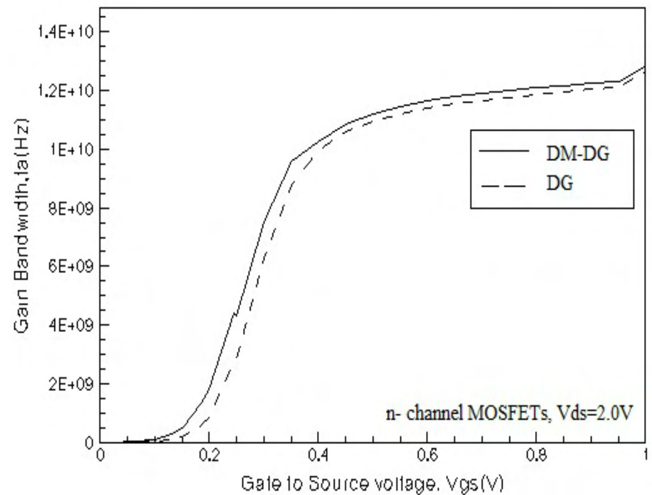

Fig.6: Comparison of the Gain bandwidth for n-channel DG and DM-DG MOSFETs as a function of gate-to-source voltage for V_{ds} = 2.0V

B.Noise performance

AC simulation is performed at equidistant bias points for small signal analysis with the gate and drain as two ports and with the source terminals grounded. The resulting small signal admittance and capacitances are used to calculate RF figure of merit. The Power spectral density of the two devices are observed at their respective drain terminals and plotted as a function of gate-to-source voltage. The proposed DM-DG device show a reduced PSD when compared with the DG device.

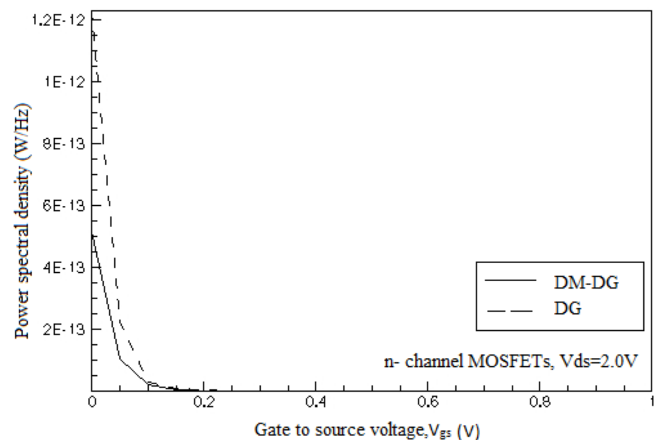

Fig.7: Comparison of noise power spectral density for n-channel DG and DM-DG MOSFETs as a function of gate-to-source voltage for V_{ds} = 2.0V.

For a general two port network Noise Figure (NF) is calculated using the following expression,

$$NF = 1 + \frac{1}{S_I^S}\left[S_I^{gg} + |\alpha^2| S_I^{dd} - 2Re(\alpha S_I^{dg})\right] \quad (3)$$

where $\alpha = (Y_s+Y_{11})/Y_{21}$, S_I^s is current noise spectrum of noisy source admittance and given by,

$$S_I^S = 4 k_B T \, Re(Y_s) \quad (4)$$

Also S_I^{gg} and S_I^{dd} are current noise spectrums at gate and drain terminals respectively. S_I^{dg} is the cross correlation current noise spectra between drain and gate terminals. We get these parameters by including appropriate models in the simulator.

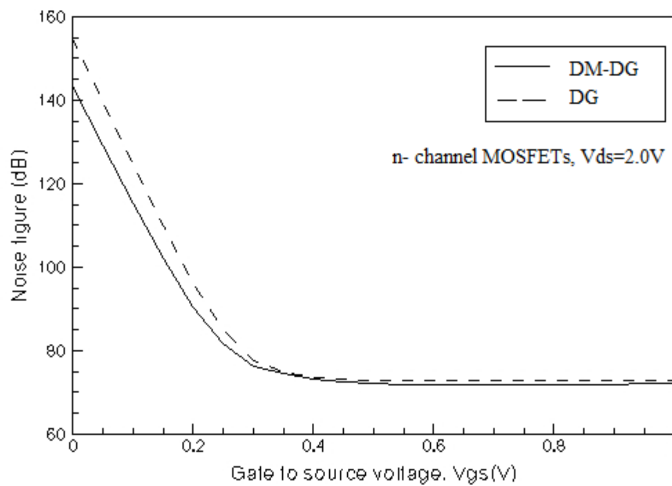

Fig.8: Comparison of the Noise figure (NF) for n-channel DG and DM-DG MOSFETs as a function of gate-to-source voltage for V_{ds} = 2.0V

Fig. 8 clearly shows that the gate engineered DM-DG improves the noise performance by reduced NF. The NF of DM-DG saturates to 70dB in saturation region i.e. $V_{gs} > V_t$.

IV. CONCLUSION

We have investigated that the gate engineered DM-DG MOSFET provide better performance than normal DG MOSFET. The increased electron mobility and velocity at channel surface due to dual gate material reduce effective electrical field at drain end, resulting in smaller DIBL and hot carrier effects. The cut-off frequency is increased by 5 GHz. Also the gain bandwidth is improved by 500MHz. The device shows better immunity towards noise as its noise figure is reduced by 2 dB. Thus it can be concluded that DMG technology is the most favorable technique for analog and RF applications.

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